St. Leger, Geoffrey

Access DB# 163960

SEARCH REQUEST FORM

Scientific and Technical Information Center

167

Requester's Full Name: Gwen Liang Examiner #: 79180 Date: 8-25-05
Art Unit: 2162 Phone Number ~~30~~ X 24038 Serial Number: 09/626,965
Mail Box and Bldg/Room Location: RND 3B-11 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: Component Management System - - -

Inventors (please provide full names): OHASHI, Tadshi

Earliest Priority Filing Date: 09/27/99 * Assignee = FUJITSU Limited

For Sequence Searches Only *Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

Concept & Background:
① To integrate the development information (including design, development, manufacture and inspection) of both hardware and firmware components into a same level of management system, stored in a hierarchical structure, using a numbering system common to both hardware and firmware development information.
② To store a meta-information about the hierarchical structure in XML
(see CON page)

Claim = 1 (focus on limitations 1-3, 1-4, 1-5)

RECEIVED
AUG 26 2005
BY:.....

* For allowance decision

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STAFF USE ONLY	Type of Search		Vendors and cost where applicable	
Searcher:	Geoffrey St. Leger	NA Sequence (#)		STN
Searcher Phone #:	03540	AA Sequence (#)		Dialog ✓
Searcher Location:	4B31	Structure (#)		Questel/Orbit
Date Searcher Picked Up:	9/8/5	Bibliographic	✓	Dr.Link
Date Completed:	9/9/5	Litigation		Lexis/Nexis
Searcher Prep & Review Time:	40	Fulltext	✓	Sequence Systems
Clerical Prep Time:		Patent Family		WWW/Internet
Online Time:	150	Other		Other (specify)

PTO-1590 (8-01)

STIC Search Report
EIC 2100

STIC Database Tracking Number: 163960

TO:	From:
Gwen Liang Location: RND 3B11 Art Unit : 2162 Friday, September 09, 2005 Case Serial Number: 09/626965	Geoffrey St. Leger Location: EIC 2100 Randolph-4B31 Phone: 23450 geoffrey.stleger@uspto.gov

Search Notes

Dear Examiner Liang,

Attached please find the results of your search request for application 09/626965. I searched Dialog's patent files, technical databases and general files.

Please let me know if you have any questions.

Regards,

Geoffrey St. Leger
4B31/x23540

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File 347:JAPIO Nov 1976-2005/Apr(Updated 050801)
         (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200557
         (c) 2005  Thomson Derwent

Set     Items   Description
S1     374694   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)(HA-
              RDWARE OR DEVICE? ? OR PARTS OR ASSEMBLIES OR SUBASSEMBLIES OR
               UNIT OR UNITS OR MACHINE? ? OR CIRCUIT? ?)
S2     119717   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)(SE-
              MICONDUCTOR? ? OR COMPONENT? ? OR COMPUTER? ? OR PC OR PCS OR
              WORKSTATION? ? OR WORK()STATION? ? OR TERMINAL? ?)
S3       5936   FIRMWARE OR FIRM()WARE OR EMBEDDED()(CHIP? ? OR MICROCHIP?
              ? OR PART? ? OR ELEMENT? ? OR MODULE? ? OR HARDWARE OR SOFTWA-
              RE OR SYSTEM? ?)
S4        233   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)S3
S5     192200   DATABASE? ? OR DATA()BASE? ? OR REPOSITOR??? OR KNOWLEDGE(-
              )BASE? ? OR KNOWLEDGEBASE? ? OR ARCHIVE? ? OR (DATA OR INFORM-
              ATION)()MANAG?????
S6     110286   HIERARCH? OR TREE? ? OR DIRECTORY OR DIRECTORIES OR FOLDER?
               ? OR NEST??? OR PARENT(1W)CHILD
S7       3637   XML OR (EXTENSIBLE OR XTENSIBLE OR EXTENDED)()(MARKUP OR M-
              ARK()UP)()LANGUAGE? ?
S8          6   S1:S2 AND S4 AND S5:S7
S9         30   S1:S2 AND S3 AND S5:S7
S10        30   S8:S9
S11         4   S10 AND AC=US/PR AND AY=(1970:1999)/PR
S12         6   S10 AND AC=US AND AY=1970:1999
S13         5   S10 AND PY=1970:1999
S14         8   S11:S13
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14/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

01974521 **Image available**
DRAWING OUTPUTTING METHOD OF PLOTTER **DRAWING** OUTPUT **DEVICE**

PUB. NO.: 61-188621 [JP 61188621 A]
PUBLISHED: August 22, 1986 (**19860822**)
INVENTOR(s): HOSHINO YOSHIHARU
APPLICANT(s): TOYO ELECTRIC MFG CO LTD [000311] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-029857 [JP 8529857]
FILED: February 18, 1985 (19850218)
INTL CLASS: [4] G06F-003/13; B43L-013/00; G06F-003/12
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1 (MISCELLANEOUS GOODS -- Office Supplies)
JOURNAL: Section: P, Section No. 535, Vol. 11, No. 12, Pg. 137, January 13, 1987 (19870113)

ABSTRACT

PURPOSE: To improve the utilization efficiency of a form by giving a drawing size data to each checkers-shaped frame formed by dividing the maximum size drawing into necessary minimum size drawings, and placing the drawing in accordance with whether a 90 deg. rotation is necessary or not.

CONSTITUTION: A titled **device** has **drawing** size data S(sub 1)-S(sub 9) in front of a plotting data, and a processing is executed by an original algorithm, by a **firmware** on a microprocessor contained in the device by said data S(sub 1)-S(sub 9). That is to say, the maximum size drawing corresponding to the corresponding table is divided, and 16 frames of frame number '0'-15 of a necessary size drawing are given to a part which has been formed on the **firmware** . Subsequently, whether the **drawing** has been placed horizontally or vertically is discriminated, and in accordance with a result of its discrimination, the respective drawings are brought to a **nesting** processing horizontally and vertically to 16 pieces of frames. By executing such a processing, a white part of a form is eliminated, and the utilization efficiency of the form is improved.

14/5/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014333153 **Image available**
WPI Acc No: 2002-153856/200220
XRPX Acc No: N02-116978
Digital information communication apparatus for computer system, has controller to determine type of trigger event and to control digital information communication between volatile and non-volatile memories
Patent Assignee: MAXTOR CORP (MAXT-N)
Inventor: LI Q; STRANG C E; ZAHORNACKY J F
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6336174	B1	20020101	US 99370855	A	19990809	200220	B

Priority Applications (No Type Date): US 99370855 A 19990809
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6336174	B1		15	G06F-012/00	

Abstract (Basic): US 6336174 B1
NOVELTY - A volatile memory (202) coupled to an information source, receives and stores digital information. A non-volatile memory (204)

receives and stores digital information communicated from the volatile memory. A controller (206) determines the type of trigger event from control information stored in the volatile memory and controls digital information communication between the memories in response to trigger event.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Memory back-up system;

(b) Computer readable medium storing memory back-up program

USE - For communicating digital information between volatile memory such as DRAM, SRAM, fast page mode DRAM, extended data out DRAM, synchronous DRAM, double-data rate SDRAM, Direct RAM-bus DRAM, Synclink DRAM, video RAM (VRAM) and window RAM (WRAM), and non-volatile memory such as flash memory, EEPROM and solid state disk, in computer system. Is also applicable to applications involved in **database** engines, peer-to-peer networks and networks that employ distributed file systems and standalone computers.

ADVANTAGE - Kernel is logically stored in the range of volatile memory and no additional software, **firmware** are needed to load the kernel, thus system boot speed is increased.

DESCRIPTION OF DRAWING(S) - The figure shows a functional block **diagram** of the **hardware** assisted memory module.

Volatile memory (202)

Non-volatile memory (204)

Controller (206)

pp; 15 DwgNo 2/5

Title Terms: DIGITAL; INFORMATION; COMMUNICATE; APPARATUS; COMPUTER; SYSTEM ; CONTROL; DETERMINE; TYPE; TRIGGER; EVENT; CONTROL; DIGITAL; INFORMATION ; COMMUNICATE; VOLATILE; NON; VOLATILE; MEMORY

Derwent Class: T01

International Patent Class (Main): G06F-012/00

File Segment: EPI

14/5/3 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013997862 **Image available**

WPI Acc No: 2001-482077/200152

XRPX Acc No: N01-356785

Tutorial information providing system redirects user actions to select commands to invoke functions of application so that functions normally performed by application are not performed, if training agent is activated

Patent Assignee: BELL J (BELL-I)

Inventor: BELL J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6219047	B1	20010417	US 98156206	A	19980917	200152	B

Priority Applications (No Type Date): US 98156206 A 19980917

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6219047	B1		9	G06F-003/00	

Abstract (Basic): US 6219047 B1

NOVELTY - A training agent (26) is activated by pressing a hot key, during which the agent redirects user actions for selecting commands to invoke functions of computer program application from application user interface so that functions normally performed by application in response to actions are not performed. The agent finds tutorial information from **database** and presents it to user in response to user actions.

DETAILED DESCRIPTION - The training agent includes no portion of the computer program application. The **database** provides a computer readable description of an application user interface and sources of computer readable tutorial information. The **database** provides linking information associating elements of the application user interface with sources of computer readable tutorial information. When the training agent is activated, it redirects the user actions for selecting commands to invoke functions of the computer program application so that functions normally performed by the application in response to the actions are not performed. Instead a presentation program is run to obtain data from **database** and to present tutorial information to the user in response to the user actions according to the computer readable description of the application user interface and linking information associating each user selected command to a source of computer readable tutorial information. INDEPENDENT CLAIMS are also included for the following:

(a) Tutorial information providing method;

(b) Computer program

USE - For providing tutorial information to a user of computer program application. Also implemented in digital electronic circuitry, or in computer hardware, software, **firmware** , etc.

ADVANTAGE - Provides a powerful, flexible and intuitive mechanism for providing tutorial information to a user of computer program. The system is implemented without affecting or requiring any reprogramming of the computer program. The system is easily configured to provide tutorial information in any format including any text, sound, video or multimedia format for which a player application exists. Provides a user of an application with training on demand. The agent provides a simple, intuitive and consisting way of retrieving help of something related to the user interface. Different tutorials are prepared for user with different level of experience. Through the agent, the user tailors the level of the detail presented by the tutorial. The tutorial content is updated without shipping new data to the user.

DESCRIPTION OF DRAWING(S) - The figure shows the block **diagram** of **computer** based system with training agent.

Training agent (26)

pp; 9 DwgNo 1/2

Title Terms: TUTOR; INFORMATION; SYSTEM; REDIRECT; USER; ACTION; SELECT; COMMAND; INVOKE; FUNCTION; APPLY; SO; FUNCTION; NORMAL; PERFORMANCE; APPLY; PERFORMANCE; TRAINING; AGENT; ACTIVATE

Derwent Class: T01; W04

International Patent Class (Main): G06F-003/00

File Segment: EPI

14/5/4 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013091750 **Image available**

WPI Acc No: 2000-263622/200023

XRPX Acc No: N00-197119

Circuit termination apparatus for terminating subscriber circuit in ATM switching system, outputs data of specified circuit and generates clock corresponding to velocity of circuit for extracting ATM cell

Patent Assignee: FUJITSU LTD (FUIT)

Inventor: KAMOI J; TADA I; YAMAGUCHI T

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000069022	A	20000303	JP 98234029	A	19980820	200023	B
US 6446146	B1	20020903	US 99296841	A	19990422	200260	

Priority Applications (No Type Date): JP 98234029 A 19980820

Patent Details:

Patent No Kind Lan Pg   Main IPC   Filing Notes
JP 2000069022 A   13 H04L-012/28
US 6446146   B1   G06F-013/00

Abstract (Basic): JP 2000069022 A
NOVELTY - A circuit switching unit (102) comprising transducers (102a,102b), specifies any one of several circuits, based on which a selector (201) outputs data of the specified circuit. Clock signal corresponding to the velocity of the specified circuit, is generated by a clock generator (202d). A common process unit (200) has **firmware** interface block (202e) for extracting ATM cell.
DETAILED DESCRIPTION - The **firmware** interface block (202e) in the common process unit, stores monitoring information in the specific area. Based on the address corresponding to the condition of monitoring information, ATM cell of the specified circuit is extracted, by a ATM cell extraction function unit (202b).
USE - Circuit termination apparatus is used for terminating the subscriber circuit accommodated in the ATM switching system and for terminating synchronous optical network (SONET) synchronous digital **hierarchy** (SDH) accommodated in ATM switching system.
ADVANTAGE - As circuit scale and external terminal are reduced, man day of **firmware** and **firmware** scale are achieved.
DESCRIPTION OF DRAWING(S) - The figure shows the block **diagram** of the **circuit** termination apparatus.
Circuit switching unit (102)
Transducers (102a,102b)
Common process unit (200)
Selector (201)
ATM cell extraction function unit (202b)
Clock generator (202d)
Firmware interface unit (202e)
pp; 13 DwgNo 2/10
Title Terms: CIRCUIT; TERMINATE; APPARATUS; TERMINATE; SUBSCRIBER; CIRCUIT; ATM; SWITCH; SYSTEM; OUTPUT; DATA; SPECIFIED; CIRCUIT; GENERATE; CLOCK; CORRESPOND; VELOCITY; CIRCUIT; EXTRACT; ATM; CELL
Derwent Class: W01; W02
International Patent Class (Main): G06F-013/00; H04L-012/28
International Patent Class (Additional): H04J-003/00; H04J-003/22; H04L-029/08; H04L-029/10; H04Q-003/00
File Segment: EPI

14/5/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012597909 **Image available**
WPI Acc No: 1999-404015/ **199934**
XRPX Acc No: N99-301053
Asynchronous transfer mode cell interface unit for high speed transmission of digital codes, video and voice in communication network
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: DANIEL T; NATTKEMPER D; VARMA S
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 5920561 A 19990706 US 96614806 A 19960307 199934 B

Priority Applications (No Type Date): US 96614806 A 19960307
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 5920561   A   37 H04L-012/56

Abstract (Basic): US 5920561 A
NOVELTY - A segmented memory holds the ATM data cells, and the

addresses indicating the data cell locations in the memory are held in registers. A processor (36) permanently pre-configured in **firmware** performs segmentation and reassembly procedures. An enhanced direct memory access (EDMA) unit (40) transfers data cells to and from the memory.

DETAILED DESCRIPTION - The processor segments the ATM data cells for storage in the respective memory segments, each of which includes a pointer, to either another memory segment containing the successive ATM data cell segment or to a null address, thus creating a linked list of memory segments. The processor also reassembles the data cells, utilizing the addresses in the registers as the initial and final element pointers of the linked list data structure. The ATM data cells include ATM conversion sub-layer protocol data units (CS-PDU). The asynchronous transfer mode cell interface (ACI) controls the memory and includes a network having a data bus.An INDEPENDENT CLAIM is also included for ATM network memory management device.

USE - For high speed transmission of digital codes, video and voice in communication network.

ADVANTAGE - The computational burden on the CPU is reduced by providing the high functionality primitives such as an interface mechanism between the hardware and software functions. The flexibility to change flow control algorithms is allowed by running a different software algorithm. By providing an ATM communication system interconnect/termination unit (ATMCSI/TU) which supports either a user defined software implemented or a default hardware implemented efficient buffer memory management scheme. The buffer memory management can be implemented on a per VC basis. By simply changing the contents of the linked list linking registers, manipulation of data in the present memory location itself is possible. As the ATMCSI/TU is provided with a **hierarchical** calender, there is reduction in memory requirements for the calender. The scheduler based traffic shaping carried out by the ATMCSI/TU reduces the CPU workload and increases the data transfer rate.

DESCRIPTION OF DRAWING(S) - The **drawing** shows organization of functional **units** of an ATMCSI/TU.

Processor (36)

EDMA unit (40)

pp; 37 DwgNo 2/17

Title Terms: ASYNCHRONOUS; TRANSFER; MODE; CELL; INTERFACE; UNIT; HIGH; SPEED; TRANSMISSION; DIGITAL; CODE; VIDEO; VOICE; COMMUNICATE; NETWORK

Derwent Class: W01

International Patent Class (Main): H04L-012/56

File Segment: EPI

14/5/6 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012525778 **Image available**

WPI Acc No: 1999-331884/ **199928**

XRPX Acc No: N99-249519

Trace control apparatus of firmware **- stores trace** data **based on trace process indication from mode register, when interruption register outputs interruption signal to** firmware

Patent Assignee: NIPPON DENKI ENG KK (NIDE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11119992	A	19990430	JP 97277806	A	19971009	199928	B

Priority Applications (No Type Date): JP 97277806 A 19971009

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11119992	A		11	G06F-009/22	

Abstract (Basic): JP 11119992 A

NOVELTY - Mode register (12) stores interruption mode data from a service processor (20). A mode register (14) stores trace process mode data from the service processor and communicates trace process signal to **firmware** . When an interruption register (13) outputs interruption signal to **firmware** (11), trace data is stored based on trace process indication of mode register. DETAILED DESCRIPTION - Hardware failure detector (15) sends hardware failure generation signal to another mode register, on hardware failure detection. When the hardware failure generation signal is output, all trace processes are stopped.

USE - For controlling input-output controller of supercomputer.

ADVANTAGE - The ability to change trace data storing area inside main memory by divided usage and occupancy usage is maintained. A lot of trace data can be extracted since trace data storing memory can be used when trace data storing area of main memory cannot be used.

DESCRIPTION OF DRAWING(S) - The figure shows the block **diagram** of **hardware** of trace control apparatus of **firmware** . (11) **Firmware** ; (12,14) Mode registers; (15) Detector; (20) Service processor.

Dwg.1/5

Title Terms: TRACE; CONTROL; APPARATUS; **FIRMWARE** ; STORAGE; TRACE; DATA; BASED; TRACE; PROCESS; INDICATE; MODE; REGISTER; INTERRUPT; REGISTER; OUTPUT; INTERRUPT; SIGNAL; **FIRMWARE**

Derwent Class: T01

International Patent Class (Main): G06F-009/22

International Patent Class (Additional): G06F-011/28

File Segment: EPI

14/5/7 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012506939 **Image available**

WPI Acc No: 1999-313044/ **199926**

XRPX Acc No: N99-233821

Utility for generating hierarchical tree **structure corresponding to power control and data control information used by BIOS**

Patent Assignee: PHOENIX TECHNOLOGIES LTD (PHOE-N)

Inventor: LEWIS T A

Number of Countries: 083 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9922295	A2	19990506	WO 98US22694	A	19981027	199926	B
AU 9912800	A	19990517	AU 9912800	A	19981027	199939	
US 5999730	A	19991207	US 97958376	A	19971027	200004	
GB 2346236	A	20000802	WO 98US22694	A	19981027	200038	
			GB 200010007	A	20000426		
JP 2001521243	W	20011106	WO 98US22694	A	19981027	200203	
			JP 2000518323	A	19981027		
GB 2346236	B	20021120	WO 98US22694	A	19981027	200301	
			GB 200010007	A	20000426		

Priority Applications (No Type Date): US 97958376 A 19971027

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9922295	A2	E	75	G06F-009/44	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9912800	A		Based on patent WO 9922295
US 5999730	A	G06F-009/45	

GB 2346236 A G06F-009/44 Based on patent WO 9922295
JP 2001521243 W 85 G06F-009/44 Based on patent WO 9922295
GB 2346236 B G06F-009/44 Based on patent WO 9922295

Abstract (Basic): WO 9922295 A2
NOVELTY - The first scope of the root of the **hierarchical tree** is defined. A bus object is attached within the first scope. The bus object corresponds to the system bus of the computer system. A second scope is defined for the bus object. A processor object is attached within the second scope of the bus object to indicate that communications to the processor of the computer system are routed via the system bus. The processor object corresponds to the processor of the computer system.
USE - The utility is for generating a **hierarchical tree** structure corresponding to power control and data control information used by BIOS. It can be used by an original equipment manufacturer (OEM) to create a graphical representation of advanced configuration and power interface (ACPI) compatible **firmware** .
ADVANTAGE - Allows alteration of configuration after boot-up. Reduces coupling between BIOS **firmware** and hardware.
DESCRIPTION OF DRAWING(S) - The drawing shows a **schematic** of an ACPI-compatible **computer** system with ACPI **firmware** .
pp; 75 DwgNo 1A/11
Title Terms: UTILISE; GENERATE; **HIERARCHY** ; **TREE** ; STRUCTURE; CORRESPOND; POWER; CONTROL; DATA; CONTROL; INFORMATION
Derwent Class: T01
International Patent Class (Main): G06F-009/44; G06F-009/45
International Patent Class (Additional): G06F-001/32
File Segment: EPI

14/5/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007195496
WPI Acc No: 1987-192505/ **198727**
XRPX Acc No: N87-144109
Software tool for automatic logic function diagram prodn. - has function blocks arranged in hierarchy **order between successive columns**
Patent Assignee: BBC BROWN BOVERI & CIE AG (BROV); SCHULT U (SCHU-I)
Inventor: SCHULT U
Number of Countries: 013 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 8703974	A	19870702	WO 86CH94	A	19860707	198727 B
EP 284605	A	19881005	EP 86904056	A	19860707	198840
JP 1500229	W	19890126	JP 86503630	A	19860707	198910
EP 284605	B	19901003				199040
DE 3674806	G	19901108				199046
US 5034899	A	19910723	US 88163117	A	19880210	199132
			US 89441215	A	19891127	

Priority Applications (No Type Date): WO 86CH94 A 19860707; EP 86904056 A 19860707; JP 86503630 A 19860707
Cited Patents: EP 200974; US 4326207; US 4445169; US 4236207
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8703974	A	G	31		
Designated States (National): JP US					
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					
EP 284605	A	G			
Designated States (Regional): CH DE FR LI SE					
EP 284605	B				
Designated States (Regional): CH DE FR LI SE					

US 5034899 A Cont of application US 88163117

Abstract (Basic): WO 8703974 A

The tool is used for prods. of a logic function diagram from a control programme for a memory programmable control on a graphic display. The function blocks are divided into columns (I.IV) from left to right using a recessive process, with the position and size of the function blocks within the columns (I.IV) by successive positioning of their inputs and outputs in that order.

The lines between the input of one function block and the output of a preceding function block are arranged horizontally at different heights. Pref. the positioning of the inputs and outputs is determined by the series sequence of the associated function blockes.

ADVANTAGE - Provides function diagrams with high data density.

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File 348:EUROPEAN PATENTS 1978-2005/Aug W04
         (c) 2005 European Patent Office
File 349:PCT FULLTEXT 1979-2005/UB=20050908,UT=20050901
         (c) 2005 WIPO/Univentio

Set     Items   Description
S1     261842   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)(HA-
              RDWARE OR DEVICE? ? OR PARTS OR ASSEMBLIES OR SUBASSEMBLIES OR
               UNIT OR UNITS OR MACHINE? ? OR CIRCUIT? ?)
S2     106360   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)(SE-
              MICONDUCTOR? ? OR COMPONENT? ? OR COMPUTER? ? OR PC OR PCS OR
              WORKSTATION? ? OR WORK()STATION? ? OR TERMINAL? ?)
S3      20755   FIRMWARE OR FIRM()WARE OR EMBEDDED()(CHIP? ? OR MICROCHIP?
              ? OR PART? ? OR ELEMENT? ? OR MODULE? ? OR HARDWARE OR SOFTWA-
              RE OR SYSTEM? ?)
S4        602   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)S3
S5     176092   DATABASE? ? OR DATA()BASE? ? OR REPOSITOR??? OR KNOWLEDGE(-
              )BASE? ? OR KNOWLEDGEBASE? ? OR ARCHIVE? ? OR (DATA OR INFORM-
              ATION)()MANAG?????
S6     129207   HIERARCH? OR TREE? ? OR DIRECTORY OR DIRECTORIES OR FOLDER?
               ? OR NEST??? OR PARENT(1W)CHILD
S7      11604   XML OR (EXTENSIBLE OR XTENSIBLE OR EXTENDED)()(MARKUP OR M-
              ARK()UP)()LANGUAGE? ?
S8          0   S1:S2(50N)S4(50N)S5(50N)S6(50N)S7
S9          1   S1:S2(100N)S4(100N)S5(100N)S6(100N)S7
S10        50   S1:S2(100N)S4(100N)S5:S7
S11        50   S9:S10
S12        20   S11 AND AC=US/PR AND AY=1970:1999/PR
S13        20   S11 AND AC=US AND AY=1970:1999
S14        11   S11 AND PY=1970:1999
S15        21   S12:S14
```

15/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01205709
Geographic data collection
Erfassung von geographischen Daten
Collecte de donnees geographiques
PATENT ASSIGNEE:
MITSUBISHI DENKI KABUSHIKI KAISHA, (208589), 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310, (JP), (Applicant designated States: all)
INVENTOR:
Akatsu, Shinji, c/o Mitsubishi Denki K.K., 2-3 Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310, (JP)
Matsubara, Fernando-Masami, 1570 Vista Club Cir.Apt. 201, Santa Clara, CA 95054, (US)
LEGAL REPRESENTATIVE:
Pfenning, Meinig & Partner (100961), Mozartstrasse 17, 80336 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1049303 A2 001102 (Basic)
EP 1049303 A3 040204
APPLICATION (CC, No, Date): EP 2000108809 000426;
PRIORITY (CC, No, Date): US 302023 990429
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H04L-029/00; G06F-003/00; H04N-007/00
ABSTRACT WORD COUNT: 179
NOTE:
Figure number on first page: NONE

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200044	1060
SPEC A	(English)	200044	9937
Total word count - document A			10997
Total word count - document B			0
Total word count - documents A + B			10997

...SPECIFICATION a functional block diagram of the home gateway of FIG. 5;
FIG. 7 is an alternate block **diagram** of the home gateway, illustrating **hardware components** ;
FIG. 8 is block **diagram** illustrating a **firmware** stack for the home gateway;
FIG. 9 depicts a protocol stack for MPEG transport over the IEEE...
...FIG. 18 depicts flowcharts pertaining to a data packet engine;
FIG. 19A-B depict a node navigation **tree** according to an embodiment of the present invention;
FIG. 19C depicts a node function list according to...

15/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01205706
Remote monitoring and control
Fernuberwachung und -steuerung
Telesurveillance et commande
PATENT ASSIGNEE:
MITSUBISHI DENKI KABUSHIKI KAISHA, (208589), 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310, (JP), (Applicant designated States: all)
INVENTOR:
Akatsu, Shinji, c/o Mitsubishi Denki K.K. 2-3 Marunouchi 2-chome,

Chiyoda-ku Tokyo 100-8310, (JP)
Miura, Shin, c/o Mitsubishi Denki K.K. 2-3 Marunouchi 2-chome, Chiyoda-ku Tokyo 100-8310, (JP)
Matsubara, Fernando Masami, 1570 Vista Club Cir. Apr. 201, Santa Clara, CA 95054, (US)
LEGAL REPRESENTATIVE:
Pfenning, Meinig & Partner (100961), Mozartstrasse 17, 80336 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1049291 A2 001102 (Basic)
EP 1049291 A3 030813
APPLICATION (CC, No, Date): EP 2000108804 000426;
PRIORITY (CC, No, Date): US 304213 990429
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H04L-012/26; H04L-012/28; H04L-012/64
ABSTRACT WORD COUNT: 136
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200044	626
SPEC A	(English)	200044	12825
Total word count - document A			13451
Total word count - document B			0
Total word count - documents A + B			13451

...SPECIFICATION a functional block diagram of the home gateway of FIG. 5;
FIG. 7 is an alternate block **diagram** of the home gateway, illustrating **hardware components** ;
FIG. 8 is block **diagram** illustrating a **firmware** stack for the home gateway;
FIG. 9 depicts a protocol stack for MPEG transport over the IEEE...

...FIG. 18 depicts flowcharts pertaining to a data packet engine;
FIG. 19A-B depict a node navigation **tree** according to an embodiment of the present invention;
FIG. 19C depicts a node function list according to...

15/3,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01091662
Electronic notebook for maintaining design information
Elektronisches Notizbuch zum Festhalten von Entwurfsdaten
Carnet de notes electronique pour preserver les donnees de conception
PATENT ASSIGNEE:
Autodesk, Inc., (2606600), 111 McInnis Parkway, San Rafael, California 94903, (US), (Proprietor designated states: all)
INVENTOR:
Bogan, William E., 14220 Jennings Vista Trail, Lakeside, California 92040, (US)
Comfort, David G., 1451 Camino Septimo, Encinitas, California 92007, (US)
Gill, David L., 13474 Appalachian Way, San Diego, California 92129, (US)
Kross, Robert L., 2924 Carriage Way, West Linn, Oregon 97068, (US)
Stark, Guri A., 50 Aaron Drive, Novato, California 94949, (US)
Wagreich, Amy B., 5015 Greenbrier Avenue, San Diego, California 92120, (US)
LEGAL REPRESENTATIVE:
Dendorfer, Claus, Dr. (85562), Wachtershauser & Hartz Tal 29, 80331 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 959421 A2 991124 (Basic)
EP 959421 A3 010307
EP 959421 B1 030730
APPLICATION (CC, No, Date): EP 99109107 990507;
PRIORITY (CC, No, Date): US 76752 980512
DESIGNATED STATES: DE; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G06F-017/50; G06T-017/40; G06T-011/60
ABSTRACT WORD COUNT: 52
NOTE:
Figure number on first page: NONE

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199947	780
CLAIMS B	(English)	200331	673
CLAIMS B	(German)	200331	659
CLAIMS B	(French)	200331	761
SPEC A	(English)	199947	6697
SPEC B	(English)	200331	6650
Total word count - document A			7478
Total word count - document B			8743
Total word count - documents A + B			16221

...SPECIFICATION that in alternate embodiments various portions of operating system 110 can be implemented in hardware and/or **firmware** . **Design** application 130 is intended to represent any of a wide variety of commercially available applications to assist...

...electrical), a structure (e.g., a house or office building), computer software, etc. According to one implementation, **design** application 130 is a **computer** -aided **design** (CAD) program, such as one of the AutoCAD(R) or Mechanical Desktop(R) family of software applications...

...from Autodesk, Inc. of San Rafael, California. However, in alternate implementations design application 130 can be other **design** products, such as a **circuit** **design** and/or simulation program, software development environment, etc. It is to be appreciated that the specific functions...

...more detail according to one embodiment of the present invention. As illustrated, electronic notebook 140 includes notebook **database** 252, main control logic 250, text view control logic 248, graphics view control logic 246, browser control...

...SPECIFICATION that in alternate embodiments various portions of operating system 110 can be implemented in hardware and/or **firmware** . **Design** application 130 is intended to represent any of a wide variety of commercially available applications to assist...

...electrical), a structure (e.g., a house or office building), computer software, etc. According to one implementation, **design** application 130 is a **computer** -aided **design** (CAD) program, such as one of the AutoCAD(R) or Mechanical Desktop(R) family of software applications...

...from Autodesk, Inc. of San Rafael, California. However, in alternate implementations design application 130 can be other **design** products, such as a **circuit** **design** and/or simulation program, software development environment, etc. It is to be appreciated that the specific functions...

...more detail according to one embodiment of the present invention. As illustrated, electronic notebook 140 includes notebook **database** 252, main control logic 250, text view control logic 248, graphics view control logic 246, browser control...

15/3,K/13 (Item 13 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00710586
FRAME STRUCTURE WHICH PROVIDES AN INTERFACE BETWEEN PARTS OF A COMPOUND DOCUMENT
RAHMENSTRUKTUR ALS SCHNITTSTELLE ZWISCHEN DEN TEILEN EINES ZUSAMMENGESETZTEN DOKUMENTS
STRUCTURE D'ENCADREMENT QUI FORME UNE INTERFACE ENTRE DES PARTIES D'UN DOCUMENT COMPOSITE
PATENT ASSIGNEE:
APPLE COMPUTER, INC., (1211954), 1 Infinite Loop,, Cupertino, CA 95014, (US), (Proprietor designated states: all)
INVENTOR:
PIERSOL, Kurt, W., 917 Pellegrini Street, Santa Cruz, CA 95062, (US)
SUSSER, Joshua, B., 111 Hammond Avenue, Santa Cruz, CA 95062, (US)
RODSETH, Richard, C., 12099 Atrium Drive, Saratoga, CA 95070, (US)
LEGAL REPRESENTATIVE:
DIEHL GLAESER HILTL & PARTNER (100237), Patentanwalte Augustenstrasse 46, 80333 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 738403 A1 961023 (Basic)
EP 738403 B1 020227
WO 9518406 950706
APPLICATION (CC, No, Date): EP 95905470 941227; WO 94US14943 941227
PRIORITY (CC, No, Date): US 175549 931230
DESIGNATED STATES: DE; GB
INTERNATIONAL PATENT CLASS: G06F-017/22; G06F-017/24
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200209	1405
CLAIMS B	(German)	200209	1307
CLAIMS B	(French)	200209	1548
SPEC B	(English)	200209	12398
Total word count - document A			0
Total word count - document B			16658
Total word count - documents A + B			16658

...SPECIFICATION how the information is displayed on the canvas of the container part It applies to all facets **nested** within the facet of interest, as well as the embedded part.
In addition to ...which areas of its Clipping Shape are translucent. A translucent area is an area in which the **embedded part** uses **drawing** results of **parts** it obscures to complete its own display. In the example of Figures 6B and 6C, the ellipse...

15/3,K/14 (Item 14 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00262652
Database access machine for factory automation.
Datenbank benutzende Maschine fur die automatische Fertigung.
Machine utilisant une base de donnees pour une usine automatique.
PATENT ASSIGNEE:
Allen-Bradley Company, (204330), 1201 South Second Street, Milwaukee Wisconsin 53204, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
Miller, William L., 803 Sun Ridge Lane, Chagrin Falls Ohio 44022, (US)

Horton, Robert E., 1713 Stonington, Hudson Ohio 44236, (US)
Hayward, Peter J., 116 E. Streetsboro, Hudson Ohio 44236, (US)
LEGAL REPRESENTATIVE:
Lippert, Hans, Dipl.-Ing. et al , Reichel und Reichel Parkstrasse 13, D-6000 Frankfurt (Main) 1, (DE)
PATENT (CC, No, Kind, Date): EP 266784 A2 880511 (Basic)
EP 266784 A3 900613
APPLICATION (CC, No, Date): EP 87116385 871106;
PRIORITY (CC, No, Date): US 928529 861107
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: G05B-019/417;
ABSTRACT WORD COUNT: 161

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	897
SPEC A	(English)	EPABF1	18229
Total word count - document A			19126
Total word count - document B			0
Total word count - documents A + B			19126

...SPECIFICATION interface functions.
The invention also enable the cell controlling computer to add or delete items from the **database** while the access machine remains "on-line" and in control of machine controlling computers. This is referred...

...the propagation of data in a control system provided by the background art;
Fig. 2 is a **hardware** -to-memory map **schematic** **diagram** of a programmable controller of a type known in the art;
Fig. 3 is a block diagram...
...of the video display of Fig. 3 as a new data item is being entered into the **database** of the access machine of Fig. 3;
Fig. 4b shows the screen of the video display of Fig. 3 as a new station record is being entered into the **database** of the access machine of Fig. 3;
Fig. 5 is a map diagram showing the relationship of certain records in the **database** maintained by the cell controlling computer and the access machine of Fig. 3;
Fig. 6 is a map diagram showing the organization of data items in a **database** residing in the access machine of Fig. 3;
Fig. 7 is a data flow diagram showing the communication of one type of **database** -related information in a system that incorporates the access machine of Fig. 3;
Fig. 8 is a data flow diagram showing the communication of another type of **database** -related information in a system that incorporates the access machine of Fig. 3;
Figs. 9-15 are maps of the **database** -related information contained in messages communicated between the cell controlling computer and the access machine in Figs. 7 and 8;
Fig. 16 is a **hardware - firmware** **schematic** showing the architecture of the access machine of Fig. 3;
Figs. 17 and 18 are block diagrams...

15/3,K/15 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00809353 **Image available**
IP LIBRARY MANAGEMENT SYSTEM
SYSTEME DE GESTION DE BIBLIOTHEQUE PAR PROTOCOLE INTERNET
Patent Applicant/Assignee:

SYNCHRONICITY SOFTWARE INC, 201 Forest Street, Marlborough, MA 01752, US, US (Residence), US (Nationality)
Inventor(s):
DEY Aparna, 1401 Red Hawk Circle, Apt. E-305, Fremont, CA 95009, US,
Legal Representative:
HEFFAN Ira V (et al) (agent), Testa, Hurwitz & Thibeault, LLP, High Street Tower, 125 High Street, Boston, MA 02110, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200142969 A2-A3 20010614 (WO 0142969)
Application: WO 2000US42299 20001128 (PCT/WO US0042299)
Priority Application: US 99456022 19991203; US 99467563 19991220
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 6962

Fulltext Availability:
Detailed Description

Detailed Description
... VCs.

can take on many forms - i.e., they can be either system level macros, megacell, or **embedded** software cores used in system chip design. VCs can generally be categorized according to the different abstro...

...IP
ID
databases or repositories have been developed to accumulate core designs for reuse.

However a mere **repository** provides no assurances that the core designs stored meet applicable standards, nor does such a **repository** necessarily provide case of and control over access and use.

1 5 Thus, there is a need for a distributed **database** providing an infrastructure for electronic design that users can access remotely and conveniently, and which provides assurances...

...I
ilize a client-server system configuration which includes a master IP system can uti I 1
database for storing virtual **component design** data, coupled to a master IP **database** server on a local area network. A catalog **database** server may also be provided on the local area network, and couples to an IP catalog **database** for storing attributes pertaining to the stored virtual component data. The IP library management system further preferably includes an IP registration system, an IP **data management** system, an IP selection system, an IP catalocr management system, and an IP modification management system, which...
...meets the standards, the IP registration system enters the new or modified data into the master IP **database** .

In a preferred embodiment, the IP management system controls whether a user may access the master IP **database** and the IP catalocr **database** .

```
File   8:Ei Compendex(R) 1970-2005/Aug W4
         (c) 2005 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2005/Aug
         (c) 2005 ProQuest Info&Learning
File  65:Inside Conferences 1993-2005/Sep W1
         (c) 2005 BLDSC all rts. reserv.
File   2:INSPEC 1969-2005/Aug W4
         (c) 2005 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2005/Jul W2
         (c)2005 Japan Science and Tech Corp(JST)
File   6:NTIS 1964-2005/Aug W4
         (c) 2005 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2005/Aug W4
         (c) 2005 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2005/Sep W1
         (c) 2005 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2005/Jul
         (c) 2005 The HW Wilson Co.
File 266:FEDRIP 2005/Jun
         Comp & dist by NTIS, Intl Copyright All Rights Res
File  95:TEME-Technology & Management 1989-2005/Jul W5
         (c) 2005 FIZ TECHNIK
File 438:Library Lit. & Info. Science 1984-2005/Jul
         (c) 2005 The HW Wilson Co

Set     Items   Description
S1     365391   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)(HA-
              RDWARE OR DEVICE? ? OR PARTS OR ASSEMBLIES OR SUBASSEMBLIES OR
               UNIT OR UNITS OR MACHINE? ? OR CIRCUIT? ?)
S2     349207   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)(SE-
              MICONDUCTOR? ? OR COMPONENT? ? OR COMPUTER? ? OR PC OR PCS OR
              WORKSTATION? ? OR WORK()STATION? ? OR TERMINAL? ?)
S3      36170   FIRMWARE OR FIRM()WARE OR EMBEDDED()(CHIP? ? OR MICROCHIP?
              ? OR PART? ? OR ELEMENT? ? OR MODULE? ? OR HARDWARE OR SOFTWA-
              RE OR SYSTEM? ?)
S4       4584   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)S3
S5     968715   DATABASE? ? OR DATA()BASE? ? OR REPOSITOR??? OR KNOWLEDGE(-
              )BASE? ? OR KNOWLEDGEBASE? ? OR ARCHIVE? ? OR (DATA OR INFORM-
              ATION)()MANAG?????
S6     929640   HIERARCH? OR TREE? ? OR DIRECTORY OR DIRECTORIES OR FOLDER?
               ? OR NEST??? OR PARENT(1W)CHILD
S7      27588   XML OR (EXTENSIBLE OR XTENSIBLE OR EXTENDED)()(MARKUP OR M-
              ARK()UP)()LANGUAGE? ?
S8        163   S1:S2 AND S4 AND S5:S7
S9        128   RD (unique items)
S10        59   S9 NOT PY=2000:2005
```

10/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05170125 E.I. No: EIP98114482285
Title: RTL design source management for system-on-a-chip designs
Author: Blaner, Bart; King, Christine; Stabler, Paul C.
Corporate Source: IBM Microelectronics, Essex Junction, VT, USA
Conference Title: Proceedings of the 1998 WESCON Conference
Conference Location: Anaheim, CA, USA Conference Date: 19980915-19980917
Sponsor: IEEE
E.I. Conference No.: 49236
Source: Wescon Conference Record 1998. Wescon, Los Angeles, CA, USA,98CB36265. p 147-152
Publication Year: 1998
CODEN: WCREDI
Language: English
Document Type: CA; (Conference Article) Treatment: G; (General Review)
Journal Announcement: 9901W3
Abstract: Increasingly, system-on-a-chip (SOC) designers are looking to leverage the expertise of design service providers to bring products to market. Design service providers may be engaged at various points in the design process: from design conception and specification to processing a completed technology-dependent netlist. Engagement typically occurs at a stage intermediate to these points; completed RTL for some portion of the design may exist but assistance is needed to integrate the RTL with other core IP, or design services may be enlisted to develop some portion of the RTL or new cores to perform specific functions. Proper management of RTL design source is critical to the overall success of a project. This paper describes a methodology used by a design service provider to address this issue. (Author abstract) 4 Refs.
Descriptors: *Integrated circuit layout; Application specific integrated **circuits** ; Logic **design** ; **Embedded systems** ; **Database** systems; Marketing; Project management; Planning
Identifiers: Register transfer level design; Project planning
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits); 721.2 (Logic Elements); 722.4 (Digital Computers & Systems); 723.3 (Database Systems); 911.4 (Marketing); 912.2 (Management)
714 (Electronic Components); 721 (Computer Circuits & Logic Elements); 722 (Computer Hardware); 723 (Computer Software); 911 (Industrial Economics); 912 (Industrial Engineering & Management)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 91 (ENGINEERING MANAGEMENT)

10/5/5 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05105999 E.I. No: EIP98084355636
Title: Automate the big bottleneck in embedded system design
Author: Gal-Oz, Shaul; Isaacs, Malcolm V.
Corporate Source: Aisys Inc, Santa Clara, CA, USA
Source: IEEE Spectrum v 35 n 8 Aug 1998. p 62-67
Publication Year: 1998
CODEN: IEESAM ISSN: 0018-9235
Language: English
Document Type: JA; (Journal Article) Treatment: G; (General Review)
Journal Announcement: 9810W4
Abstract: Testing for bugs during the hardware and software integration phase is presently the root problem in designing embedded systems and is closedly followed by the cost of finding and eliminating these bugs. The DriveWay 3DE (**device** driver **design** environment) provides a **hardware**

-independent application programming interface (API) for the **design** of **embedded systems** and is about eight times as fast as a manual approach. It automatically builds fully tested drivers and boot code, and it does away with a prime source of errors and misunderstanding by fully documenting the work. It is a key piece of automation for software and hardware integration, founded as it is on **knowledge base** , user-interface with the **knowledge base** , and a set of test functions.

Descriptors: *Embedded systems; Computer architecture; User interfaces; Program debugging; Microprocessor chips; **Knowledge based** systems; Real time systems; Computer programming; Computer operating systems; Network protocols

Identifiers: Application programming interface (API); **Device** driver **design** environment (3DE); Real time operating systems (RTOS); High level data link control (HDLC) protocols

Classification Codes:

723.4.1 (Expert Systems)

722.2 (Computer Peripheral Equipment); 723.1 (Computer Programming); 723.4 (Artificial Intelligence)

722 (Computer Hardware); 723 (Computer Software); 721 (Computer Circuits & Logic Elements)

72 (COMPUTERS & DATA PROCESSING)

10/5/6 (Item 6 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

05005044 E.I. No: EIP98044175175

Title: HiPART: A new hierarchical semi-interactive HW-/SW partitioning approach with fast debugging for real-time embedded systems

Author: Hollstein, Thomas; Becker, Juergen; Kirschbaum, Andreas; Glesner, Manfred

Corporate Source: Darmstadt Univ of Technology, Darmstadt, Ger

Conference Title: Proceedings of the 1998 6th International Workshop on Hardware/Software Codesign

Conference Location: Seattle, WA, USA Conference Date: 19980315-19980318

Sponsor: IEEE

E.I. Conference No.: 48270

Source: Hardware/Software Codesign - Proceedings of the International Workshop 1998. IEEE Comp Soc, Los Alamitos, CA, USA,98TB100232. p 29-33

Publication Year: 1998

CODEN: 85PQAI

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 9806W4

Abstract: In this contribution we present a new system-level hardware/software partitioning approach (HiPART) which is run in the frame of an integrated **hardware** software **design** methodology for **embedded system design** . The benefits of the approach result from an **hierarchical** partitioning algorithm, consisting of three phases of constructive and iterative methods. The main advantage of the system is a freely selectable degree of user interaction and manual partitioning. A permanent observation of timing constraint violations during partitioning guarantees the applicability for real-time systems. (Author abstract) 12 Refs.

Descriptors: *Computer architecture; Distributed computer systems; **Hierarchical** systems; Algorithms; Iterative methods; Interactive computer systems; Real time systems; Computer debugging; Software engineering

Identifiers: System level hardware/software partitioning

Classification Codes:

921.6 (Numerical Methods); 722.4 (Digital Computers & Systems); 723.1 (Computer Programming)

722 (Computer Hardware); 723 (Computer Software); 921 (Applied Mathematics)

72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

10/5/9 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04840761 E.I. No: EIP97103848645
Title: Tools for documenting digital designs on the Web
Author: Borriello, Gaetano; Beal, Douglas; Li, Tianyu
Corporate Source: Univ of Washington, Seattle, WA, USA
Conference Title: Proceedings of the 1997 IEEE International Conference on Microelectronic Systems Education, MSE'97
Conference Location: Arlington, VA, USA Conference Date: 19970721-19970723
Sponsor: IEEE
E.I. Conference No.: 47027
Source: Proceedings of the IEEE International Conference on Microelectronic Systems Education, MSE 1997. IEEE, Los Alamitos, CA, USA,97TB100127. p 7-8
Publication Year: 1997
CODEN: 002680
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); G ; (General Review)
Journal Announcement: 9711W4
Abstract: Modern **embedded system designs** include elements described using **schematics** , **hardware** description languages, timing **diagrams** , and various programming languages. We have developed a set of Java applets that facilitate the documentation of designs for dissemination over the web. These tools enable the specification of multiple layers of active regions on diagrams and on text so that different mouse-over comments and/or hyper-text links can be attached to elements on each layer. This layering supports multiple **hierarchical** views of the same design. The tools, thus provide a highly expressive and modular system for navigating design documentation. These same tools can be used to provide a medium for delivering comments on students' work. We would expect such functionality to eventually be directly supported by EDA tool vendors. (Author abstract)
Descriptors: *Digital integrated **circuits** ; **Computer** aided **design** ; Data communication systems; Wide area networks; Information use; Information dissemination; Engineering education; Computer hardware description languages
Identifiers: Electronic design automation (EDA)
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits); 723.5 (Computer Applications); 722.3 (Data Communication, Equipment & Techniques); 903.3 (Information Retrieval & Use); 903.2 (Information Dissemination); 901.2 (Education)
714 (Electronic Components); 723 (Computer Software); 722 (Computer Hardware); 903 (Information Science); 901 (Engineering Profession)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 90 (GENERAL ENGINEERING)

10/5/10 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04741769 E.I. No: EIP97073727136
Title: Knowledge representation in MICKEY: an expert system for designing microprocessor-based systems
Author: Mitra, Raj S.; Basu, Anupam
Corporate Source: Indian Inst of Technology, Kharagpur, India
Source: IEEE Transactions on Systems, Man, and Cybernetics Part A:Systems and Humans v 27 n 4 July 1997. p 467-479
Publication Year: 1997

CODEN: ITSHFX ISSN: 1083-4427
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)
Journal Announcement: 9708W4
Abstract: This paper presents the knowledge representation schemes adopted in MICKEY, a **knowledge based** system for designing microprocessor based systems. MICKEY is essentially a hybrid expert system, using rules and procedures for achieving the different design tasks. We briefly describe the **hierarchy** of tasks in this problem domain, and emphasize on the refinement paradigm, constraint propagation, conflict resolution and task management strategies adopted in MICKEY. Next, we dwell upon the different knowledge sources and their functions, with respect to the particular design domain. Finally, we present an industrial design, achieved by MICKEY, to demonstrate its applicability. (Author abstract) 27 Refs.
Descriptors: *Knowledge representation; Expert systems; **Computer** aided **design** ; Microcomputers; **Knowledge based** systems; **Computer hardware** ; Computer software; Concurrent engineering
Identifiers: Microprocessor based systems; Real time **embedded systems** ; Industrial **design**
Classification Codes:
723.4.1 (Expert Systems)
723.4 (Artificial Intelligence); 723.5 (Computer Applications); 722.4 (Digital Computers & Systems); 723.1 (Computer Programming); 913.6 (Concurrent Engineering)
723 (Computer Software); 722 (Computer Hardware); 913 (Production Planning & Control)
72 (COMPUTERS & DATA PROCESSING); 91 (ENGINEERING MANAGEMENT)

10/5/11 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04122185 E.I. No: EIP95032641079
Title: Specification and design **of** embedded hardware **-software systems**
Author: Gajski, Daniel D.; Vahid, Frank
Corporate Source: Univ of California, Irvine, CA, USA
Source: IEEE Design & Test of Computers v 12 n 1 Spring 1995. p 53-67
Publication Year: 1995
CODEN: IDTCEC ISSN: 0740-7475
Language: English
Document Type: JA; (Journal Article) Treatment: G; (General Review)
Journal Announcement: 9505W5
Abstract: Designing an embedded-system involves creating a specification of the system's functionality and mapping that functionality for implementation by a set of processors, ASICs, memories and buses. This tutorial discusses the key problems of system specification and design, including specification capture, **design** exploration, **hierarchical** modeling, software and **hardware** synthesis, and co-simulation. Existing tools and methods for solving these problems are presented. Also described is a 'specify-explore-refine' methodology that can lead to substantial productivity gains through the early detection of functional errors and through faster exploration of design alternatives. 47 Refs.
Descriptors: *Computer systems; Specifications; Computer software; Systems analysis; Computer hardware; Computer simulation; Software engineering; **Hierarchical** systems; Fuzzy sets; Electric control equipment
Identifiers: Embedded hardware software systems; System functionality; Cosimulation; State minimization; Fuzzy logic controller
Classification Codes:
722.4 (Digital Computers & Systems); 902.2 (Codes & Standards); 723.5 (Computer Applications); 723.1 (Computer Programming); 732.1 (Control Equipment)

722 (Computer Hardware); 902 (Engineering Graphics & Standards); 723 (Computer Software); 732 (Control Devices)
72 (COMPUTERS & DATA PROCESSING); 90 (GENERAL ENGINEERING); 73 (CONTROL ENGINEERING)

10/5/16 (Item 16 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02108121 E.I. Monthly No: EIM8608-050690
Title: DESIGN **AND SPECIFICATION OF MICROPROGRAMMED** COMPUTER **ARCHITECTURES.**
Author: Damm, Werner
Corporate Source: RWTH, Aachen, West Ger
Conference Title: Proceedings - 18th Annual Workshop on Microprogramming, MICRO 18.
Conference Location: Pacific Grove, CA, USA Conference Date: 19851203
Sponsor: ACM, Special Interest Group on Microprogramming, New York, NY, USA; IEEE Computer Soc, Technical Committee on Microprogramming, Los Alamitos, CA, USA; EUROMICRO
E.I. Conference No.: 08013
Source: MICRO: Annual Microprogramming Workshop 18th. Publ by ACM, New York, NY, USA. Available from IEEE Service Cent (Cat n 85CH2232-7), Piscataway, NJ, USA p 3-9
Publication Year: 1985
CODEN: MAWMDB ISSN: 0361-2163 ISBN: 0-89791-172-5
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8608
Abstract: A **hierarchical firmware design** method is presented, to structure a microprogrammed level of a computer architecture into independently verifiable modules. Specifications of the system are given in axiomatic architecture description language (AADL). The design and specification style is illustrated using an emulation example. 28 refs.
Descriptors: *COMPUTER ARCHITECTURE--*Microprogramming; COMPUTER PROGRAMMING LANGUAGES
Identifiers: **HIERARCHICAL FIRMWARE DESIGN** METHOD; AXIOMATIC ARCHITECTURE DESCRIPTION LANGUAGE; AADL
Classification Codes:
723 (Computer Software); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING)

10/5/17 (Item 17 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02076211 E.I. Monthly No: EIM8603-013554
Title: APPROACH TO DESIGN-FOR-MAINTENANCE.
Author: Silverman, Jon; Giddings, Nancy; Beane, John
Corporate Source: Honeywell Systems & Research Cent, Minneapolis, MN, USA
Conference Title: Record - Software Maintenance Workshop.
Conference Location: Monterey, CA, USA Conference Date: 19831206
Sponsor: IEEE Computer Soc, Technical Committee on Software Engineering, Los Alamitos, CA, USA.; NBS, Gaithersburg, MD, USA.; Naval Postgraduate School, Monterey, CA, USA.
E.I. Conference No.: 07691
Source: Publ by IEEE, New York, NY, USA Available from IEEE Service Cent (Cat n 83CH1982-8), Piscataway, NJ, USA p 106-110
Publication Year: 1984
ISBN: 0-8186-0510-3
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8603

Abstract: Maintenance of a software system is enhanced when a software architecture is viewed as an interconnection of parts. A Component Interconnection Language (CIL) has been defined for representing software architectures. In addition, several structural complexity metrics have been defined for evaluating architectures. The CIL supports maintenance in four basic ways: as a vehicle for recording design history, by helping a maintainer evaluate the effect of proposed design change, by aiding design retesting procedures, and as a basis for **knowledge - based** assistants for design and maintenance. The CIL and metrics have been evaluated in a **design** of a selected real-time, **embedded software** system. 14 refs.

Descriptors: *COMPUTER SOFTWARE--* **Design** ; MAINTENANCE; **COMPUTER** SYSTEMS PROGRAMMING; **COMPUTER** SYSTEMS, DIGITAL--Real Time Operation; COMPUTER ARCHITECTURE

Identifiers: COMPONENT INTERCONNECTION LANGUAGE; **KNOWLEDGE - BASED** ASSISTANTS

Classification Codes:
723 (Computer Software); 913 (Production Planning & Control); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING); 91 (ENGINEERING MANAGEMENT)

10/5/18 (Item 18 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02046423 E.I. Monthly No: EI8611106840 E.I. Yearly No: EI86023607

Title: AADL/S* APPROACH TO FIRMWARE DESIGN **VERIFICATION.**

Author: Damm, Werner; Doehmen, Gert; Merkel, Klaus; Sichelschmidt, Mathilde

Corporate Source: RWTH, Aachen, West Ger

Source: IEEE Software v 3 n 4 Aug 1986 p 27-37

Publication Year: 1986

CODEN: IESOEG ISSN: 0740-7459

Language: ENGLISH

Document Type: JA; (Journal Article) Treatment: T; (Theoretical)

Journal Announcement: 8611

Abstract: It is shown how a complete **firmware design** (ranging from specification of the image architecture, and formal description of the microarchitecture, to a **hierarchically** organized high-level microprogram) can be formalized using AADL/S* languages. Techniques underlying support tools for interactive design steps are outlined. In particular, it is demonstrated that design verification can be automatically carried out based on AADL/S* design representation. The AADL/S* approach to **firmware design** was successfully tested in an emulation case study involving commercially available image and target architectures. 13 refs.

Descriptors: *COMPUTER SOFTWARE--* **Design** ; **COMPUTER ARCHITECTURE** -- Microprogramming

Identifiers: MICROARCHITECTURE; **FIRMWARE DESIGN**

Classification Codes:
723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

10/5/21 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01629103 ORDER NO: AAD98-21661

HARDWARE /SOFTWARE CO- DESIGN OF HETEROGENEOUS REAL-TIME DISTRIBUTED EMBEDDED SYSTEMS **(SOFTWARE)**

Author: DAVE, BHARAT PURUSHOTTAM

Degree: PH.D.

Year: 1998

Corporate Source/Institution: PRINCETON UNIVERSITY (0181)

Source: VOLUME 59/01-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 344. 262 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0544

There has been an explosive growth and interest in embedded system development. Embedded system applications range from consumer appliance, such as microwave ovens, hand-held cellular phones, and multimedia systems, to large telecom systems employing thousands of processors. Embedded systems used in power-sensitive applications, such as mobile communications, demand low power systems, whereas embedded systems employed in critical applications demand high reliability and availability. This thesis presents a suite of techniques which takes an embedded system specification, specified in terms of acyclic task graphs, as input, and automatically produces a low-cost heterogeneous distributed system architecture meeting system constraints.

Emphasis on distributed **embedded system** architecture co- **design** and partitioning is fairly recent. Two distinct approaches have been used to solve the distributed system co-design problem: optimal and heuristic. Optimal approaches are suitable only for small task graphs consisting of 10 or so tasks. This thesis presents the first work to address very large tasks graphs (with over 2,100 tasks).

In this thesis, we introduce five **hardware** /software co- **design** systems: (1) COSYN, (2) COSYN-LP, (3) COFTA, (4) COHRA, and (5) CASPER. The emphasis of COSYN and COSYN-LP is on general and low-power embedded systems. Fault-tolerant distributed systems can offer high performance as well as reliability and availability to meet the needs of critical real-time applications. COFTA optimizes the architecture for fault tolerance during co-design. Traditional non- **hierarchical** architectures create communication and processing bottlenecks, and are impractical for medium-to-large systems. Such systems require a large number of processing elements and communication links connected in a **hierarchical** manner, thus forming a **hierarchical** distributed architecture. To address this problem we introduce the concepts of task and communication delegation. We propose a co-design system called COHRA to optimize the architecture **hierarchy** . COHRA also supports the notion of **hierarchical** task graphs encountered in medium-to-large scale embedded systems.

Embedded system specifications also contain some aperiodic task graphs which have real-time constraints. We propose a **hardware** /software co- **design** system called CASPER, which addresses concurrent **hardware** /software co- **design** of periodic and aperiodic **embedded system** functions.

The efficacy of the proposed algorithms and techniques have been demonstrated on real-life telecom transport systems with a large number of examples.

10/5/28 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

05952589 INSPEC Abstract Number: C9507-6110J-004
Title: Visually designing embedded-systems applications
Author(s): Drusinsky, D.
Journal: Dr. Dobb's Journal vol.20, no.6 p.62, 64, 66, 68, 104-6
Publication Date: June 1995 Country of Publication: USA
CODEN: DDJSDM ISSN: 1044-789X
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Because it enables code reuse and enhances maintenance, inheritance is one of the more-important properties of object oriented programming. In a C++ implementation of firmware for a product such as a digital answering machine, for instance, one base (parent) program can perform operating-system-like routines (storing/deleting messages), while the other performs push-button and keypad control. With C++, different answering machines can inherit and enhance these classes, thereby leading

to specific versions of answering- **machine firmware** . Also, the parent **designs** can be reused in many other designs, without requiring intimate familiarity with the original parent design. In the authors' article (Extended State Diagrams and Reactive Systems, ibid., October, 1994), the author introduced the concept of extended state diagrams and illustrated their applicability for the design and development of reactive systems, which react to inputs that are not ready at any given point in time. Extended state diagrams (ESDs) are conventional finite state diagrams (FSDs) augmented with **hierarchy** (the ability to draw states inside states and do top-down design), concurrency (the ability to describe independent and conceptually concurrent threads of control inside any state), and visual synchronization (the ability to visually describe dependencies between these threads). In short, ESDs are the visual counterpart of an enhancement of FSMs. ESDs address the limitations of traditional state diagrams, while retaining their visual and intuitive appeal. (0 Refs)
Subfile: C
Descriptors: C language; C listings; firmware; object-oriented programming; real-time systems
Identifiers: C; C++ listing; real time system; microcode; firmware; embedded-systems application; visually designing; inheritance; object oriented programming; digital answering machine; operating-system-like routine; extended state diagrams; finite state diagram; reactive system; **hierarchy** ; concurrency; visual synchronization; multithreading; ESD
Class Codes: C6110J (Object-oriented programming); C5140 (Firmware); C6140D (High level languages); C6110P (Parallel programming)

10/5/36 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02615242 JICST ACCESSION NUMBER: 96A0203447 FILE SEGMENT: JICST-E
A Design Method For Systems By Modeling Of Extended Finite State Machine.
KONO ZEN'YA (1); FAR B H (1)
(1) Saitama Univ., Fac. of Eng.
Joho Shori Gakkai Kenkyu Hokoku, 1996, VOL.96,NO.6(SE-107), PAGE.113-120, FIG.7, REF.8
JOURNAL NUMBER: Z0031BAO ISSN NO: 0919-6072
UNIVERSAL DECIMAL CLASSIFICATION: 681.3.02.001 007.52.001
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper reports on a high quality **design** method for **embedded systems** by modeling of Finite State **Machine** (FSM). A high quality **design** requires a systematic design procedure. This method details a system, a FSM, and then it is decomposed to Extended Finite State Machines(EFSM's). At the high level design, the FSM is decomposed by data flow dividing, it is partitioned to **hierarchical** EFSM's. Using Message Sequence Chart, state transition diagrams are derived, then they are systematically detailed leading to final source codes. In order to achieve a high quality design, design steps are recorded in small steps, and checked carefully and rigorously. It is expected that ppm order quality may be achieved. The idea in this paper is found useful for Object Oriented Design. (author abst.)
DESCRIPTORS: computer system development; finite state machine; computation model; quality expansion; object oriented programming; documentation; software design; diagram and table; state transition diagram
BROADER DESCRIPTORS: development; sequential machine; automaton; model; quality assurance; assurance; computer programming; **information management** ; management; design
CLASSIFICATION CODE(S): JD02010R; JB04000O

10/5/37 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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01514493 JICST ACCESSION NUMBER: 92A0040680 FILE SEGMENT: JICST-E
Design **Procedures for** Embedded Systems **used for Hardware Control and Communications.**
KONO ZEN'YA (1)
(1) Saitama Univ., Faculty of Engineering
Joho Shori Gakkai Kenkyu Hokoku, 1991, VOL.91,NO.99(PRG-5), PAGE.107-116, FIG.11, REF.25
JOURNAL NUMBER: Z0031BAO ISSN NO: 0919-6072
UNIVERSAL DECIMAL CLASSIFICATION: 681.3.02.001
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes **design** procedures for **embedded systems** with sequential nature and used for hardware control and communications. In developments of such systems, systems **design** , software **design** and **hardware design** go on interacting with each other. Key factors for good design are quite the same in these three. After showing several key factors, design procedures starting from systems **design** , software **hardware** partitioning and software **design** with sequentialnature. The design procedures for the runtime system is also described. Throughout the paper, it is emphasizedthat following are key factors for high quality design: Clarify design procedures for each small design steps, Leave design records or documents at each small design steps and Careful checks based on them. (author abst.)
DESCRIPTORS: computer system development; software engineering; computer architecture; software design; system interface; **hierarchical** structure; exchange control system; message switching; **hardware design**
BROADER DESCRIPTORS: development; engineering; computer system(architecture); method; design; interface; structure; control system(computer); store-and-forward switching; communication exchanging ; exchange; switching
CLASSIFICATION CODE(S): JD02010R

10/5/39 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS
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1749077 NTIS Accession Number: PB93-882868
Firmware : Design **Techniques and Applications. (Latest citations from the INSPEC: Information Services for the Physics and Engineering Communities** Database)
(Published Search)
NERAC, Inc., Tolland, CT.
Corp. Source Codes: 103588000
Sponsor: National Technical Information Service, Springfield, VA.
Aug 93 250 citations
Languages: English Document Type: Bibliography
Journal Announcement: GRAI9320
Updated with each order. Supersedes PB92-860451. Sponsored in part by National Technical Information Service, Springfield, VA.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC N01/MF N01
Country of Publication: United States
The bibliography contains citations concerning the **design** , evaluation, and applications of **computer firmware** . Firmware construction, testing,

verification, and maintenance are discussed. Applications in direct digital control, process control, signal and image processing, microcomputer systems, and microprocessor systems are presented. (Contains 250 citations and includes a subject term index and title list.)
Descriptors: *Bibliographies; *Microprogramming; Computer programming; Computer software
Identifiers: *Firmware; Published Searches; NTISNTISH; NTISNERACD
Section Headings: 62B* (Computers, Control, and Information Theory--Computer Software); 88E (Library and Information Sciences--Reference Materials)

10/5/40 (Item 3 from file: 6)
DIALOG(R)File 6:NTIS

1538126 NTIS Accession Number: PB91-102525
Acquisition and Reuse of Knowledge to Design Embedded Software
Seppaenen, V.
Valtion Teknillinen Tutkimuskeskus, Espoo (Finland).
Corp. Source Codes: 067526000
Report No.: VTT/PUB-66; ISBN-951-38-3579-0
c1990 230p
Languages: English
Journal Announcement: GRAI9101
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A11/MF A02
Country of Publication: Finland
A framework for acquiring software design knowledge is presented and an interactive advisory system to reuse that knowledge. The focus is on a particular type of design expertise, called navigation knowledge. Such knowledge is needed to guide the software design process. Addressed are technical issues of which design goals to achieve, what design operators to apply next and how to perform design operations, what kinds of knowledge are needed to navigate, how this knowledge is acquired and what methods are effective for its reuse. Existing knowledge engineering and design tracking techniques are applied to build a problem space for software design and to capture navigation knowledge for searching it. The authors present an organization for the design knowledge centered around a set of generic software construction tasks and an architecture of a **knowledge - based** assistant system to reuse navigation knowledge.
Descriptors: ***Compute** r software; Embedding; **Design**
Identifiers: *Foreign technology; *Software engineering; * **Knowledge based** systems; *Reusable software; * **Computer** systems **design** ; Real time; **Computer** architecture; NTISTFTISF
Section Headings: 62B (Computers, Control, and Information Theory--Computer Software)

10/5/43 (Item 6 from file: 6)
DIALOG(R)File 6:NTIS

1474263 NTIS Accession Number: PB90-122342
Software Development Trends
Uuspaeae, P. ; Mononen, J.
Valtion Teknillinen Tutkimuskeskus, Espoo (Finland).
Corp. Source Codes: 067526000
Report No.: VTT/SYMPOSIUM-104; ISBN-951-38-3495-6
c1989 391p
Languages: English Document Type: Conference proceeding
Journal Announcement: GRAI9003

Presented at the Joint Finnish-Soviet Software Symposium held in Helsinki, Finland, on November 15-17, 1988.

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NTIS Prices: PC A17/MF A03

Country of Publication: Finland

The Proceedings volume, Software Development Trends, includes the papers presented at the Symposium. The papers have been organized into eight sessions, with following titles: **Design** of Distributed and **Embedded Systems** ; **Computer** Aided Software Engineering; Language and Interface Design; **Knowledge Based** Systems; Software Industry; Software Technology for CAD and CASE; Realtime Software Development; and Algorithms. (Copyright (c) Valtion teknillinen tutkimuskeskus (VTT) 1989.)

Descriptors: *Meetings; *Software engineering; Computer programming; Systems engineering; Algorithms

Identifiers: *Foreign technology; *Computer software; Distributed computer systems; Expert systems; **Knowledge bases** (Artificial intelligence); **Computer** aided **design** ; Real time systems; NTISTFTISF

Section Headings: 62B* (Computers, Control, and Information Theory--Computer Software); 62GE (Computers, Control, and Information Theory--General)

10/5/52 (Item 3 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05657412 Genuine Article#: WN929 Number of References: 137

Title: Design **of** embedded systems **: Formal models, validation, and synthesis**

Author(s): Edwards S (REPRINT) ; Lavagno L; Lee EA; SangiovanniVincentelli A

Corporate Source: UNIV CALIF BERKELEY,DEPT ELECT ENGN & COMP SCI/BERKELEY//CA/94720 (REPRINT); CADENCE BERKELEY LABS,/BERKELEY//CA/94704

Journal: PROCEEDINGS OF THE IEEE, 1997, V85, N3 (MAR), P366-390

ISSN: 0018-9219 Publication date: 19970300

Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394

Language: English Document Type: REVIEW

Geographic Location: USA

Subfile: CC ENGI--Current Contents, Engineering, Computing & Technology

Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC

Abstract: This paper addresses the **design** of reactive real-time **embedded systems** . Such systems are often heterogeneous in implementation technologies and **design** styles, for example by combining **hardware** application-specific integrated circuits (ASIC's) with **embedded software** . The concurrent **design** process for such **embedded systems** involves solving the specification, validation, and synthesis problems. We review the variety of approaches to these problems that have been taken.

Identifiers--KeyWord Plus(R): REAL-TIME SYSTEMS; HARDWARE-SOFTWARE CODESIGN; AUTOMATA; CIRCUITS; LUSTER

Research Fronts: 95-6100 002 (PETRI NETS; FLEXIBLE MANUFACTURING SYSTEMS; MODELING BIOLOGICAL PATHWAYS)

95-0063 001 (FORMAL SEMANTICS; INTEGRATED SOFTWARE ENVIRONMENT)

95-0118 001 (PATH DELAY-FAULT TESTABILITY; BINARY DECISION DIAGRAMS; BOOLEAN FUNCTIONS; PARTIAL SCAN **DESIGN** ; TESTABLE SEQUENTIAL- **CIRCUITS** ; ATPG PERFORMANCE)

95-1434 001 (OBJECT-ORIENTED SYSTEMS; INTELLIGENT **DATABASE DESIGN** ; SPREADSHEET MODELING; **COMPUTER** ALGEBRA)

95-2485 001 (OPERATIONAL SEMANTICS FOR TIMED CSP; DISTRIBUTED SYSTEMS; BISIMULATION EQUIVALENCE; ACTION REFINEMENT; IMPLEMENTATION OF

STOY JE, 1977, DENOTATIONAL SEMANTI
SUHLER PA, 1990, V9, J PRALLEL DISTRIB SY
SUTARWALA S, 1994, P INT WORKSH HARDW S
SUZUKI K, 1996, P DES AUT C
TAKACH A, 1995, V44, P1, IEEE T COMPUT
TENHAGEN K, 1993, P INT WORKSH HARDW S
THEISSINGER M, 1994, P INT WORKSH HARDW S
THOMAS DE, 1993, V10, P6, IEEE DES TEST COMPUT
TIWARI V, 1994, V2, P437, IEEE T VLSI SYST
VAHID F, P DES AUT C JUN 1992
VALMARI A, 1992, V1, P297, FORMAL METHODS SYST
VONDERBEECK M, 1984, V863, P128, LNCS
VOSS M, 1994, P INT WORKSH HARDW S
WADGE W, 1985, LUCID DATAFLOW PROGR
WALKUP E, 1993, P INT WORKSH HARDW S
WILBERG J, 1994, P INT WORKSH HADW S
WILSON J, 1994, P INT WORKSH HARDW S

10/5/54 (Item 5 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01025742 Genuine Article#: FP616 Number of References: 0
(NO REFS KEYED)
Title: AN INTEGRATED MULTICOMPUTER DSS DESIGN FOR TRANSPORT PLANNING USING EMBEDDED COMPUTER -SIMULATION AND DATABASE TOOLS
Author(s): COCHRAN JK; CHEN MT
Corporate Source: ARIZONA STATE UNIV,SYST SIMULAT LAB/TEMPE//AZ/85287
Journal: DECISION SUPPORT SYSTEMS, 1991, V7, N2, P87-97
Language: ENGLISH Document Type: ARTICLE
Geographic Location: USA
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: COMPUTER APPLICATIONS & CYBERNETICS
Abstract: Goods movement is probably the most neglected issue in transport planning. What work has been done is largely restricted to urban goods movement. A major project funded by the Arizona Department of Transportation has resulted in a unique Decision Support System for transportation planners of highway goods movement. This paper presents the design of that system. Some of the system's unique features include: (1) use of both mainframe and microcomputers to form an integrated interface, (2) use of a **database** language to organize and preprocess mail survey data and topology data, and (3) use of a discrete-event computer simulation model to perform "what-if" scenanarios in a statistically valid manner. All components of the system are accessed through a user-friendly menu structure which assists in both data manipulation and the translation of simulation experiment output into summaries of commodity type, weight distribution, capacity analysis, safety implications, and pavement maintenance. This DSS, named AFNA (Arizona Freight Network Analysis), is the first involving simultaneous embedded computer simulation and **database** tools. It is complete and now in use providing ADOT transportation engineers with new planning capabilities.
Descriptors--Author Keywords: **COMPUTER** SIMULATION; DSS **DESIGN** ; **EMBEDDED SOFTWARE** TOOLS; TRANSPORT PLANNING; MULTICOMPUTER DSS; HIGHWAY GOODS MOVEMENT

10/5/58 (Item 4 from file: 266)
DIALOG(R)File 266:FEDRIP

00426458
IDENTIFYING NO.: 0132780 AGENCY CODE: NSF

CAREER: Structured Design **of** Embedded Software
PRINCIPAL INVESTIGATOR: De Alfaro, Luca
PERFORMING ORG.: University of California-Santa Cruz, Computer Engineering, Santa Cruz, CA 95064-1077
PROJECT MONITOR: Gill, D. Helen
SPONSORING ORG.: National Science Foundation, CCR, 4201 Wilson Boulevard , Arlington, Virginia 22230
DATES: 20020101 TO 20021231 FY : 2002 FUNDS: $320,000 (300000)
SUMMARY: Embedded software is ubiquitous: it is present in a vast array of everyday products and appliances, and it accounts for an increasing share of the functionality and development cost of systems such as cars and aircrafts. Innovation in many fields, from transportation to military, from consumer products to manufacturing, is increasingly dependent on our ability to **design** ever more sophisticated **embedded systems** . Yet, the sophistication and complexity of embedded software is fast approaching the limit of current design abilities. This project aims at developing a formal approach to **embedded software design** that copes with complexity through the exploitation of design structure, and in particular, of modularity (the ability to assemble a system from components) and **hierarchy** (the ability to implement a complex component as a collection of simpler components). The project is articulated in three directions. The first project direction focuses on methods and tools for ensuring that the **components** used in a **design** are compatible one with the other. This helps to avoid bugs stemming from the interaction of multiple components, which are often among the hardest to prevent and detect. The project develops theories of component interfaces that captures the protocol, timing, and performance aspects of the interaction among embedded software components. The resulting interface theories constitute an extended type system that encompasses not only the values passed as inputs and outputs, but also the dynamic behavior of the **components** , enabling to check at **design** time whether the **components** interact in a compatible way. The second project direction investigates methods for deriving the performance and reliability of a system from that of its components. In parallel to this modular approach to analysis, this project direction will pursue a modular approach to debugging, in which the components are analyzed in isolation, and the results are used to guide the simulation of the entire system. Finally, as embedded systems are often used as controllers of a device or physical system, the third project direction proposes the use of multi-modal stochastic systems, a model that supports in an integrated fashion system identification, controller design, and code generation.

10/5/59 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00565130 I91110809937
Architecture for an embedded secure data base **management system**
(Architektur fuer ein Datenbankverwaltungssystem mit integrierter Datensicherung)
Irvine, CE; Schell, RR; Vetter, LL
Gemini Comput. Inc., Carmel, CA, USA
Proceedings of the Sixth Annual Computer Security Applications Conference, 3-7 Dec. 1990, Tucson, AZ, USA1990
Document type: Conference paper Language: English
Record type: Abstract
ISBN: 0-8186-2105-2

ABSTRACT:
The architecture for an embedded secure **database** management system (ESDBMS) applicable to C(exp 3) environments is presented. The ESDBMS **design** consists of three major **components** : the GEMSOS tamperproof security kernel, an embedded system run-time executive and the trusted ORACLE RDBMS. The ESDBMS is designed to support a fully-functional DBMS while meeting high assurance requirements. Future enhancements to the basic

version of the ESDBMS are identified which will broaden its applicability.
DESCRIPTORS: **DATABASE** MANAGEMENT SYSTEM; BACK UP; SUPERVISORY PROGRAMS; DATA INTEGRITY

File 256:TecInfoSource 82-2005/Sep
(c) 2005 Info.Sources Inc

Set	Items	Description
S1	739	(DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)(HARDWARE OR DEVICE? ? OR PARTS OR ASSEMBLIES OR SUBASSEMBLIES OR UNIT OR UNITS OR MACHINE? ? OR CIRCUIT? ?)
S2	889	(DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)(SEMICONDUCTOR? ? OR COMPONENT? ? OR COMPUTER? ? OR PC OR PCS OR WORKSTATION? ? OR WORK()STATION? ? OR TERMINAL? ?)
S3	714	FIRMWARE OR FIRM()WARE OR EMBEDDED()(CHIP? ? OR MICROCHIP? ? OR PART? ? OR ELEMENT? ? OR MODULE? ? OR HARDWARE OR SOFTWARE OR SYSTEM? ?)
S4	32	(DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)S3
S5	12145	DATABASE? ? OR DATA()BASE? ? OR REPOSITOR??? OR KNOWLEDGE()BASE? ? OR KNOWLEDGEBASE? ? OR ARCHIVE? ? OR (DATA OR INFORMATION)()MANAG?????
S6	3904	HIERARCH? OR TREE? ? OR DIRECTORY OR DIRECTORIES OR FOLDER? ? OR NEST??? OR PARENT(1W)CHILD
S7	4011	XML OR (EXTENSIBLE OR XTENSIBLE OR EXTENDED)()(MARKUP OR MARK()UP)()LANGUAGE? ?
S8	3	S1:S2 AND S4 AND S5:S7

8/5/1
DIALOG(R)File 256:TecInfoSource

01104469 DOCUMENT TYPE: Product

PRODUCT NAME: FASTPATH Software (104469)

LVL7 Systems Inc (725137)
13000 Weston Pkwy #105
Cary, NC 27513 United States
TELEPHONE: (919) 865-2703

RECORD TYPE: Directory

CONTACT: Sales Department

LVL7 Systems' FASTPATH (TM) Software is a design system for companies that build switching, routing, routing, and access devices. FASTPATH Software integrates with networks processors and networking ASICs. The system includes applications, protocols, interfaces, and management features. FASTPATH Software supports development across multiple operating systems. Users can customize its features. FASTPATH Switching includes 802.1D, spanning **tree** , flow control GARP, GVRP, GMRP applications and protocols. It includes BootP, DHCP, XMODEM, TFTP, and other system functions. FASTPATH Software's FASTPATH Routing module supports RIP 1 and 2, OSPF 2, VRRP, and other features. FASTPATH Multicast, which works with FASTPATH Routing, offers multicast packet controls. FASTPATH Management includes a command line interface and Web-based management features. FASTPATH Software also includes the FASTPATH Traffic Services and FASTPATH Bandwidth Provisioning components. FASTPATH Traffic Services supports MPLS, Diff Serv, and RSVP-TE protocols. The bandwidth-provisioning component lets systems administrators allocate bandwidth according to user demand.

DESCRIPTORS: Bandwidth Management; **Circuit Design** ; Communications Interfaces; Electrical Engineering; Electronics; **Embedded Systems** ; Network Software; Software Marketing

HARDWARE: Hardware Independent; IBM PC & Compatibles
OPERATING SYSTEM: Linux; Proprietary Operating Environment
PROGRAM LANGUAGES: Not Available
TYPE OF PRODUCT: Micro; Workstation
POTENTIAL USERS: Network Equipment Design and Planning, Network Software Design
PRICE: Available upon request

REVISION DATE: 20020930

8/5/2
DIALOG(R)File 256:TecInfoSource

00151992 DOCUMENT TYPE: Review

PRODUCT NAMES: Gladiator CLD (223101)

TITLE: CLD combines FPGA technology with ASIC logic
AUTHOR: Fuller, Meghan
SOURCE: Portable Design, v10 n2 p40(1) Feb 2004
ISSN: 1086-1300
HOMEPAGE: http://www.portabledesign.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis

GRADE: Product Analysis, No Rating

Leopard Logic Gladiator, a family of configurable logic devices (CLDs), integrates field programmable gate array (FPGA) technology with hard-wired ASIC logic. Gladiator devices give system designers the advantages of ASIC and FPGA abilities, including improved performance, higher density, lower power requirements, and lower per-unit costs of conventional FPGAs. CLDs also have a rapid design cycle and faster time to volume than ASICs, which means a reduced non-recurring engineering (NRE) cost. The devices are field- upgradeable through embedded FPGAs. The Gladiator CLD can be easily customized for specific market segments or customers through the implementation of high-speed logic in the mask-programmable area of the device. Customers send their generated configuration data to Leopard Logic; the samples are delivered to customers within weeks. Leopard Logic has patented HyperBlox FP and MP fabrics, which are the foundation of the Gladiator CLDs. The SRAM-based FP fabric is based on Leopard's proprietary HyperRoute FPGA technology, which uses a fully **hierarchical** , multiplexer-based, point-to-point interconnect. Gladiator CLDs include an FPGA-similar design flow that reduces the long timing closure cycles related to cell-based ASICs, gate arrays, and structured ASICS. With the integration of Leopard's ToolBlox suite of development tools and design kits, customers can use extant infrastructure and design methodologies.

COMPANY NAME: Leopard Logic Inc (756652)
SPECIAL FEATURE: Charts
DESCRIPTORS: CAE; **Circuit Design** ; Electrical Engineering; **Embedded Systems** ; Intelligent Controllers
REVISION DATE: 20041100

8/5/3

00146921 DOCUMENT TYPE: Review

PRODUCT NAMES: Codesign (806951); Embedded Systems (830390)

TITLE: Taking on the Embedded System Design **Challenge**
AUTHOR: Henkel, Jorg Hu, Xiaobo Sharon Bhattacharyya, Shuvra S
SOURCE: IEEE Computer, v36 n4 p35(3) Apr 2003
ISSN: 0018-9162
HOMEPAGE: http://computer.org/computer

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

We are entering a new era of synthesis tools that are the impetus for integration of **hardware** and software **components** during system **design** and development. **Hardware** /software codesign implies the methodology, tools, and practices supporting integration of hardware and software components and in the past concentrated only on **computer** -aided **design** methods, but now affects most facets of **embedded system design** . The more integrated **design** approach is changing process scheduling communication protocols, code generation, and software development environments and has led to new ways of designing application-specific processes and reconfigurable and customizable architectures . Progress over the last ten years is discussed. The creation of a virtual product with all associated subsystems, along with testing and verification before manufacturing, is appealing because to shortens time to market and lowers costs. Today's researchers want to build a unified path to genuine hardware/software codesign. Among topics covered are system definitions, design styles, and platform-based design. Developers operate on the assumption that all blocks and interfaces are verified before release, but

keeping the platform correct as architecture changes occur is a major and continuous effort in verification and new standard setting. Engineers can now do derivative system-on-chip (SoC) design with a good architecture and a stringent **hierarchical** design methodology by replacing cores. Platform-based **design** is a good choice for **embedded software** but is only a temporary solution for SoC designs.

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File 275:Gale Group Computer DB(TM) 1983-2005/Sep 08
         (c) 2005 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2005/Sep 09
         (c) 2005 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2005/Sep 08
         (c) 2005 The Gale Group
File  16:Gale Group PROMT(R) 1990-2005/Sep 08
         (c) 2005 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2005/Sep 09
         (c)2005 The Gale Group
File 624:McGraw-Hill Publications 1985-2005/Sep 09
         (c) 2005 McGraw-Hill Co. Inc
File  15:ABI/Inform(R) 1971-2005/Sep 09
         (c) 2005 ProQuest Info&Learning
File 647:CMP  Computer Fulltext 1988-2005/Aug W3
         (c) 2005 CMP Media, LLC
File 674:Computer News Fulltext 1989-2005/Sep W1
         (c) 2005 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2005/Sep 07
         (c) 2005 Dialog
File 369:New Scientist 1994-2005/Jun W2
         (c) 2005 Reed Business Information Ltd.
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 610:Business Wire 1999-2005/Sep 09
         (c) 2005 Business Wire.

Set     Items   Description
S1     331642   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)(HA-
              RDWARE OR DEVICE? ? OR PARTS OR ASSEMBLIES OR SUBASSEMBLIES OR
               UNIT OR UNITS OR MACHINE? ? OR CIRCUIT? ?)
S2     542665   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)(SE-
              MICONDUCTOR? ? OR COMPONENT? ? OR COMPUTER? ? OR PC OR PCS OR
              WORKSTATION? ? OR WORK()STATION? ? OR TERMINAL? ?)
S3     132853   FIRMWARE OR FIRM()WARE OR EMBEDDED()(CHIP? ? OR MICROCHIP?
              ? OR PART? ? OR ELEMENT? ? OR MODULE? ? OR HARDWARE OR SOFTWA-
              RE OR SYSTEM? ?)
S4      12876   (DRAWING? ? OR SCHEMATIC? ? OR BLUEPRINT? ? OR DIAGRAM? ? -
              OR SKETCH OR SKETCHES OR DESIGN? ? OR ILLUSTRATION? ?)(5N)S3
S5    2880148   DATABASE? ? OR DATA()BASE? ? OR REPOSITOR??? OR KNOWLEDGE(-
              )BASE? ? OR KNOWLEDGEBASE? ? OR ARCHIVE? ? OR (DATA OR INFORM-
              ATION)()MANAG?????
S6    1276758   HIERARCH? OR TREE? ? OR DIRECTORY OR DIRECTORIES OR FOLDER?
               ? OR NEST??? OR PARENT(1W)CHILD
S7     170258   XML OR (EXTENSIBLE OR XTENSIBLE OR EXTENDED)()(MARKUP OR M-
              ARK()UP)()LANGUAGE? ?
S8        169   S1:S2(50N)S4(50N)S5:S7
S9         17   S1:S2(50N)S4(50N)S5(50N)S6:S7
S10        53   S1:S2(20N)S4(20N)S5:S7
S11        55   S9:S10
S12        35   RD (unique items)
S13        27   S12 NOT PY=2000:2005
```

13/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02014407 SUPPLIER NUMBER: 18895253 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Storage management solutions for distributed computing environments. (HP's OpenView OmniBack II, OpenView OmniBack II for Workgroups and OpenView OmniStorage storage management software) (Product Information)
Lomb, Reiner; Emo, Kelly A.; VanDoorn, Roy M.
Hewlett-Packard Journal, v47, n5, p81(9)
Oct, 1996
ISSN: 0018-1153 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 9583 LINE COUNT: 00808

... and implementation and conducted research on compensation and reliability. Professionally interested in **databases** , workflows, and telecommunications, he has authored over twenty conference and journal publications on compilers, software engineering, and **database** and workflow systems. Weimin is married and has two children.
Qiming Chen...

...integration, multilayer workflow system architecture, and commit control and failure recovery of **nested** transactions and business processes. Currently he is working on HP's OpenPM...
...authored over fifty technical publications in journals, books, and international conferences on **databases** , **knowledge bases** , logic programming, and software engineering.
77 Agent Tester Toolkit
Paul A. Stoecker 1986 he held a number of **hardware** and **firmware design** positions on various products including the HP 9845 and HP 9000 workstations...

13/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01723360 SUPPLIER NUMBER: 16314507 (USE FORMAT 7 OR 9 FOR FULL TEXT)
DDS-2 tape autoloader: high-capacity data storage in a 5.25-inch form factor. (HP C1553A DDS-2 DAT tape autoloader) (includes related articles on the autoloader's control electronics and firmware design)
Dimond, Steven A.
Hewlett-Packard Journal, v45, n6, p12(8)
Dec, 1994
ISSN: 0018-1153 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 6773 LINE COUNT: 00511

... 13.
Mechanism and Drive Firmware. This development effort is described in "Autoloader **Firmware Design** " on page 15.
Mechanical **Design** Methods
ME30, HP's 3D **computer** -aided **design** tool, was used by the mechanical and manufacturing engineers. It was run...

...HP 9000 Series 700 workstations that had a common disk mounted with **directories** structured and named like the product subassemblies. The designers were responsible for...

13/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01680067 SUPPLIER NUMBER: 15328958 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Literature watch.

Microprocessor Report, v8, n5, p22(1)
April 18, 1994
ISSN: 0899-9341 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 793 LINE COUNT: 00066

... EDN, 3/3/94, p. 121, 3 pp.
PC-based EDA-tool **directory** . Workstation-based tools are being challenged by a broad range of software...

...embedded systems grow more complex, designers turn to increasingly sophisticated tools. (Includes **directory** of debuggers for **embedded systems** .) Jeff Child, **Computer Design** , 3/94, p. 105, 6 pp.
Halsim--a very fast SPARC V9...

...of VHDL. The future of VHDL is to build productive, cost-effective **design** tools. Dr. Allen Dewey, IBM; **Computer Design** , 3/94, p. 129, 3 pp.
DSPs
EDA tools zero in on...
...Computer Architure News, 3/94, p.44, 7 pp.
The state of **knowledge** . **based** systems. **Knowledge - based** systems can assist human operators by autonomously making decisions in complex systems...

13/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2005 The Gale Group. All rts. reserv.

01635895 SUPPLIER NUMBER: 15119636 (USE FORMAT 7 OR 9 FOR FULL TEXT)
ESDA boosts CAE technology to higher levels. (electronic system design automation; computer-aided engineering)(includes related articles on system-level design tools and graphical and textual design)
Maliniak, Lisa
Electronic Design, v41, n25, p61(7)
Dec 2, 1993
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 4259 LINE COUNT: 00358

... interactor tool incorporates configurable elements called actors that can be built into **hierarchies** . Users create analysis and verification views from the actors that are tuned...

...Sparc processor model running a C program.
TD Technologies' Transcend addresses concurrent **hardware** and software **design** with virtual execution of **embedded software** on the system model. This is supported by linking actual software code...

13/3,K/5 (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2005 The Gale Group. All rts. reserv.

01319441 SUPPLIER NUMBER: 07928662 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Indistinguishable from magic. (Editor's Notes) (column)
Hildebrand, J.D.
Computer Language, v6, n11, p5(2)
Nov, 1989
DOCUMENT TYPE: column ISSN: 0749-2839 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 1016 LINE COUNT: 00083

... articles available on the authors' BBS--it's strictly for contributors to **COMPUTER** LANGUAGE, AI Expert, **Database** Programming & **Design** , **Embedded Systems** Programming, UNIX Review, and LAN Magazine.

Finally: rush out and get a...

13/3,K/6 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01255618 SUPPLIER NUMBER: 06701432 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Linking case to testing and development tools. (MicroCase Inc.)
Milne, Bob
Electronic Design, v36, n21, p173(3)
Sept 22, 1988
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1051 LINE COUNT: 00087

... results back in the Teamwork environment on a Sun 3 or 386i **workstation** (Fig. 1).
Before examining the **design** -verification link in greater detail, a look at the tools being linked...

...real-time extensions. It's mainly aimed at designers of real-time **embedded systems** . Teamwork's **design database** includes information describing the relationships between the modules that make up a...

13/3,K/7 (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

02132106 Supplier Number: 55289730 (USE FORMAT 7 FOR FULLTEXT)
Centura's RDM/Vx Chosen As Embedded Database For New Internet-Enabled Set-Top Boxes.
Business Wire, p0393
July 28, 1999
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 625

... RDM/Vx design win strengthens Centura's position as leading vendor of **database** management technology for intelligent Internet **devices** and **embedded systems**
In a **design** win reinforcing Centura Software's (NASDAQ:CNTR) leading position in **data management** for intelligent Internet devices and embedded systems, Centura's Raima **Database** Manager for VxWorks (RDM/Vx) has been chosen as the embedded **database** for a new generation of intelligent set-top boxes to be used...

13/3,K/8 (Item 2 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01234557 Supplier Number: 44168830 (USE FORMAT 7 FOR FULLTEXT)
New Hobbit Family Personal Communicator Chip Sets Offer Performance, Power, and Integration Options
News Release, pN/A
Oct 18, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1182

... systems also include PenPoint binaries, and a symbolic debugger.
To debug their **hardware** and **firmware designs** , OEMs can turn to the
ICD, which provides ICE-like capabilities, or...a run- time library

(with floating point emulation software), assembler, and linker- **archiver** . The software development tools can be hosted on 386- and 486-based...

13/3,K/9 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2005 The Gale Group. All rts. reserv.

02482180 Supplier Number: 44979542 (USE FORMAT 7 FOR FULLTEXT)
A&T WINS NUWC CONTRACT (SEPT 7/2211 GMT)
Periscope Daily Defense News Capsules, pN/A
Sept 7, 1994
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 131

... include periscopes, antennas, communications, and electronic support measures (ESM). Work will include **design** and fabrication of **hardware** , **firmware** , and software; training; engineering and technical support for dockside and at-sea...

...trouble-shooting, and repair; among other tasks.
(COPYRIGHT 1994, PERISCOPE/USNI MILITARY **DATABASE** . FOR MORE INFORMATION CALL GREG BEAUDOIN, 1-800-929-4824, EXT 365...

13/3,K/10 (Item 2 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2005 The Gale Group. All rts. reserv.

01241143 Supplier Number: 41282641 (USE FORMAT 7 FOR FULLTEXT)
Software.
Navy News & Undersea Technology, v7, n15, pN/A
April 16, 1990
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 145

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...the Boeing Production Management System into its plant, and the contractor would **design** the **hardware** , software and **firmware** for the station. Specifically, the contractor would do analysis of existing or planned **information management** and processing capabilities, preparation of detailed program specifications, development and coding and debugging of **databases** and programs, preparation of system user and operation manuals, evaluation and maintenance...

13/3,K/11 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2005 The Gale Group. All rts. reserv.

06441712 Supplier Number: 55009255 (USE FORMAT 7 FOR FULLTEXT)
Configurable processors readied for SoC.(system-on-chip design)(Technology Information)
Rowen, Chris
Electronic Engineering Times, p98
June 28, 1999
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1189

... code size and die size, as well as power dissipation.

In this **design** scheme, the embedded-system engineer uses a processor generator to create one...

...specific instructions.
These new configurable-processor technologies come at a time when **hardware** and software co- **design** plays an increasing role in embedded-system design. The embedded- **system** designer gradually evolves the system concept from an abstract representation, often in...

...correct integration of all the systems as they undergo detailed design.
A **hierarchy** of partitioning is central to co-design. Part of this involves identifying...

...a certain level of embedded design productivity. Designers perform most of the **hardware** **design** using **hardware** -description languages (HDLs) like Verilog or VHDL. Or they reuse previously developed...

...operating systems (RTOSes).
However, the industry is undergoing significant changes that affect **embedded** - **system** **design** and the requirements placed on co-design. More designs combine advanced user...

...number of gates and bytes of code used in next generations of **embedded** **systems** .
These emerging co- **design** issues are best handled by improving the range of choices in the partitioning and implementation of the system's **hardware** and software **design** . More latitude is needed by the designer to verify that all the...

...efficiency of a design by extending the instruction-set architecture specifying memory **hierarchy** characteristics (instruction RAM and cache, data RAM and cache), bus interfaces and...

13/3,K/12 **(Item 2 from file: 16)**

06225004 Supplier Number: 54234154 (USE FORMAT 7 FOR FULLTEXT)
Analog IP critical for system design.(System-on-a-chip)(Technology Information)
Chang, Henry
Electronic Engineering Times, p80(1)
March 29, 1999
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1185

... system codesign. Given a functional model, this step partitions and maps the **design** to **hardware** and software **components** based on an IP **database** or on a better-qualified set of IP found in an application-specific integration platform. **Hardware** **design** is performed via a **hierarchical** block-based methodology. Care must be taken to plan the chip with...

...party IP blocks are "collared" to add suitable interfaces for the SOC. **Embedded** **software** **design** follows a similar methodology. Throughout the core-design process, a complex verification...
...streaming for verification.
Design for manufacturing test (DFT) is critical to the **hardware** **design** of the blocks. The isolated nature of the IP blocks, the inclusion ...

13/3,K/13 **(Item 3 from file: 16)**

DIALOG(R)File 16:Gale Group PROMT(R)

05283227 Supplier Number: 48046937 (USE FORMAT 7 FOR FULLTEXT)
Tool users set to sound off
Goering, Richard
Electronic Engineering Times, p50
Oct 13, 1997
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 471

... investigate, and how you'd like to use the Internet in your **design** work. **Embedded software** -development tools are included as a category.
While you're there, check out a new EDTN feature called "Hot Tools." It is a **directory** that lets you quickly find vendors in any given tool category. When you go into this **directory** , you'll first see a listing of categories, such as PCB **Design** , Formal Verification, **Hardware** /Software Virtual Prototyping, Libraries and many others.
Clicking on any category brings...

13/3,K/14 (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04567393 Supplier Number: 46713599 (USE FORMAT 7 FOR FULLTEXT)
Design Software
Electronic News (1991), p32
Sept 16, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1716

... support.
Aisys Ltd. formed Aisys Inc. in Santa Clara, Calif., to bring **design** automation to the **embedded systems** market and announced Driveway 3DE comprising: Chip Resource Navigator, with a unified view of the processor and maintaining the **hierarchy** of the selections made by the designer; API Library Selector, where the user configures the device drivers library to meet the needs of the **design** ; Peripheral Configuration manager, setting **hardware** preferences and adapts driver code to those settings; On-line Guides, with...

13/3,K/15 (Item 5 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

02705293 Supplier Number: 43614113 (USE FORMAT 7 FOR FULLTEXT)
Miller-Freeman Forges into IT Publishing, Trade Shows
Business Marketing, p39
Feb, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 521

... Star.
Other Miller-Freeman high tech titles include Unix Review, Al Expert **Database** Programming & **Design** , Mathematica Journal, **Embedded Systems** Programming, Printed **Circuit** Fabrication, Printed **Circuit Design** and **Circuits** Assembly.
Its technology trade shows include Dexpo, Software Development Conference and Exposition...

13/3,K/16 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2005 The Gale Group. All rts. reserv.

10631752 SUPPLIER NUMBER: 20650942 (USE FORMAT 7 OR 9 FOR FULL TEXT)
ADI Awarded BEACON System Integration Services Contract For Automotive Chassis Control Software
PR Newswire, p529DEF020
May 29, 1998
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 387 LINE COUNT: 00038

... BEACON is a productivity tool that allows an engineer to specify an **embedded software design** using **hierarchical** block **diagrams** . BEACON then automatically converts these diagrams into source code, and generates the **unit** test vectors. Also, BEACON exports **design** diagrams to a document preparation system to produce high-quality documentation. BEACON...

13/3,K/17 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2005 The Gale Group. All rts. reserv.

07598119 SUPPLIER NUMBER: 15998020 (USE FORMAT 7 OR 9 FOR FULL TEXT)
MILLER FREEMAN LAUNCHES COMMUNICATION SYSTEMS DESIGN
PR Newswire, p1219SF002
Dec 19, 1994
LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 407 LINE COUNT: 00038

... working synergistically with the other magazines in our Electronics Publishing Division, including **Embedded Systems** Programming, Printed **Circuit Design** , Printed **Circuit** Fabrication, LAN Magazine, and Stacks: The Network Journal."
Miller Freeman also publishes...

...s Journal, CADENCE Magazine, OS/2 Magazine, UNIX Review, Software Development, DBMS, **Database** Programming & Design, The Mathematica Journal, AutoCAD Tech Journal, OS/2 Developer, AI...

13/3,K/18 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2005 The Gale Group. All rts. reserv.

06809767 SUPPLIER NUMBER: 14347763 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Miller Freeman: cleared for takeoff. (Miller Freeman Publications Inc.) (Company Profile)
Isler, Erika
Folio: the Magazine for Magazine Management, v22, n12, p56(4)
July 1, 1993
DOCUMENT TYPE: Company Profile ISSN: 0046-4333 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 3150 LINE COUNT: 00249

... s Journal * The Microsoft Systems Journal. MIS/DP: Steve Schneiderman. LAN Magazine * **Database** Programming & **Design** * Stacks * DBMS. ELECTRONICS: Ted Bahr. **Circuits** Assembly * **Embedded Systems** Programming * Printed **Circuit Design** * Printed **Circuit** Fabrication * Cadence. INTERNATIONAL: Pete May, a sales-rep organization representing overseas magazines...

13/3,K/19 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00376633 87-35467
Machine-Independent Microprogram Address Allocation Through Hierarchical Structuring
Isoda, Sadahiro
Microprocessing & Microprogramming v19n4 PP: 291-304 Oct 1987
ISSN: 0165-6074 JRNL CODE: EUJ

...ABSTRACT: classes. It structures the microinstructions in a microprogram into a 3-level **hierarchy** in conformance with multiway jump restrictions. The algorithm has been applied to the compiler of a **computer** -aided **firmware design** system called CHEF (Conversational and **Hierarchical** languages system for Enhanced Firmware). The results of a preliminary assessment demonstrate...

13/3,K/20 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00312158 86-12572
Verification of Microprogram Transformation Commands for a Firmware Editor (Revised)
Isoda, Sadahiro
Microprocessing & Microprogramming v17n2 PP: 61-76 Feb 1986
ISSN: 0165-6074 JRNL CODE: EUJ

...ABSTRACT: been implemented in a firmware editor which is a subsystem of a **computer** -aided **firmware design** system, Conversational and **Hierarchical** languages system for Enhanced Firmware (CHEF). Evaluation of time performance of the...

13/3,K/21 (Item 3 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00271360 85-11793
Hands and Minds Across the Sea/The E10-FIVE Design
Stone, Roger B.
Telephony v208n6 (Part 2) PP: 18-21 Feb 11, 1985
ISSN: 0040-2656 JRNL CODE: TPH

...ABSTRACT: a switch for the US market. It was developed with US-specific **hardware** , **firmware** , and software **designs** . After extensive testing, the final testing stage for the switch was held...

...E10-FIVE's reconfigurable distributed architecture can be easily integrated into the **hierarchy** of the direct distance dialing network. It also can accommodate the latest...

13/3,K/22 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01194963 CMP ACCESSION NUMBER: EET19990628S0076
Configurable processors readied for SoC
Chris Rowen, President, Chief Executive Officer, Tensilica Inc., Santa Clara, Calif.
ELECTRONIC ENGINEERING TIMES, 1999, n 1067, PG98
PUBLICATION DATE: 990628

JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: System Design - Focus: Configurable Platforms
WORD COUNT: 1202

... code size and die size, as well as power dissipation.

In this **design** scheme, the embedded-system engineer uses a processor generator to create one...

...specific instructions.

These new configurable-processor technologies come at a time when **hardware** and software co- **design** plays an increasing role in embedded-system design. The embedded- **system** designer gradually evolves the system concept from an abstract representation, often in...
...correct integration of all the systems as they undergo detailed design.

A **hierarchy** of partitioning is central to co-design. Part of this involves identifying...

...a certain level of embedded design productivity. Designers perform most of the **hardware design** using **hardware** -description languages (HDLs) like Verilog or VHDL. Or they reuse previously developed...

...operating systems (RTOSes).

However, the industry is undergoing significant changes that affect **embedded - system design** and the requirements placed on co-design. More designs combine advanced user...

...number of gates and bytes of code used in next generations of **embedded systems** .

These emerging co- **design** issues are best handled by improving the range of choices in the partitioning and implementation of the system's **hardware** and software **design** . More latitude is needed by the designer to verify that all the...

...efficiency of a design by extending the instruction-set architecture specifying memory **hierarchy** characteristics (instruction RAM and cache, data RAM and cache), bus interfaces and...

13/3,K/23 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01188128 CMP ACCESSION NUMBER: EET19990329S0063
Analog IP critical for system design
Henry Chang, Services R&D Architecture Group, Cadence Design Systems, San Jose, Calif.
ELECTRONIC ENGINEERING TIMES, 1999, n 1054, PG80
PUBLICATION DATE: 990329
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: System Design - Focus: System-On-A-Chip
WORD COUNT: 1192

... system codesign. Given a functional model, this step partitions and maps the **design** to **hardware** and software **components** based on an IP **database** or on a better-qualified set of IP found in an application-specific integration platform. **Hardware design** is performed via a **hierarchical** block-based methodology. Care must be taken to plan the chip with...

...party IP blocks are " collared" to add suitable interfaces for the SOC. **Embedded software design** follows a similar methodology. Throughout the core-design process, a complex verification...
...streaming for verification.

Design for manufacturing test (DFT) is critical to the **hardware design** of the blocks. The isolated nature of the IP blocks, the inclusion ...

13/3,K/24 (Item 3 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2005 CMP Media, LLC. All rts. reserv.

01141341 CMP ACCESSION NUMBER: EET19971013S0055
Tool users set to sound off (Desktop Engineering)
Richard Goering
ELECTRONIC ENGINEERING TIMES, 1997, n 975, PG50
PUBLICATION DATE: 971013
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Design
WORD COUNT: 469

... investigate, and how you'd like to use the Internet in your **design** work. **Embedded software** - development tools are included as a category.
While you're there, check out a new EDTN feature called "Hot Tools. " It is a **directory** that lets you quickly find vendors in any given tool category. When you go into this **directory** , you'll first see a listing of categories, such as PCB **Design** , Formal Verification, **Hardware** /Software Virtual Prototyping, Libraries and many others.
Clicking on any category brings...

13/3,K/25 (Item 4 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2005 CMP Media, LLC. All rts. reserv.

00535172 CMP ACCESSION NUMBER: EET1993021 5S5462
Expansion leads to openings at Cyrix, Dell - Cyrix to hire four for new design center (Where The Jobs Are)
ELECTRONIC ENGINEERING TIMES, 1993, n 733, 59
PUBLICATION DATE: 930215
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: The Profession
WORD COUNT: 477

... at Dell include test manager, MCAD manager, product-planning manager, PC architect, **firmware / device** -driver engineers, electronics **design** engineers and **PC** power engineers.
While not all positions require bachelor's degrees, all call for two to six years' experience in related fields of **PC design** . Apple needs OO DB, Lisp developers
Cambridge, Mass. - Apple Computer Inc. has openings for a senior object-oriented **database** scientist and a senior Lisp/Scheme scientist at its Cambridge R&D...

13/3,K/26 (Item 1 from file: 810)
DIALOG(R)File 810:Business Wire
(c) 1999 Business Wire . All rts. reserv.

0391571 BW368

MILLER FREEMAN: Miller Freeman Inc. hosts ultimate pit stop on information superhighway; Software Development and Business Software Solutions conferences will give birth to tomorrow's software

March 14, 1994

Byline: Business Editors & Computer Writers

...2 Developer, OS/2 Magazine, Microsoft Systems Journal, Software Development, Unix Review, **Database** Programming & Design, DBMS, LAN, Stacks: The Network Journal, Cadence, Circuits, Assembly, **Embedded Systems** Programming, Printed **Circuit Design** and Printed **Circuit** Fabrication.
Headquartered in San Francisco, Miller Freeman Inc. is one of the...

13/3,K/27 (Item 2 from file: 810)
DIALOG(R)File 810:Business Wire

0260867 BW003

CHIPS AND TECHNOLOGIES: CHIPS and Technologies seeks M/PAX architecture buyer

January 21, 1992

Byline: Business Editors and Computer Science Writers

...features a message-based 128-bit wide internal data bus in a **directory** -based write back multi-processing implementation.
To date, multi-processing UNIX ports...

...PAX hardware consists of five VLSI components. These are:
o 92C390 Cache **Directory** Comparator
o 92C392 System Control Unit Memory Controller
o 92C393 DMA Controller...

...operating system porting expertise for systems.
M/PAX assets for sale include **design** and **semiconductor** manufacturing **databases** , rights to patents and other intellectual property, software, and other items related...

...solutions incorporating the SuperState System Management Architecture, CHIPSets, software accelerators, networking solutions, **firmware** , and **design** services.

St. Leger, Geoffrey

Access DB# _____

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: Gwen Liang Examiner #: 79180 Date: 8-25-05
Art Unit: 2162 Phone Number ~~30~~ X 24038 Serial Number: 09/626,965
Mail Box and Bldg/Room Location: RND 3B-11 Results Format Preferred (circle): (PAPER) DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: Component Management System - - -

Inventors (please provide full names): OHASHI, Tadshi

Earliest Priority Filing Date: 09/27/99 * Assignee = FUJITSU Limited

For Sequence Searches Only ***Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.***

Concept & Background:
① To integrate the development information (including design, development, manufacture and inspection) of both hardware and firmware components into a same level of management system, stored in a hierarchical structure, using a numbering system common to both hardware and firmware development information.
② To store a meta-information about the hierarchical structure in XML
(see CON page)

Claim = 1 (focus on limitations 1-3, 1-4, 1-5)

* For allowance decision

****

STAFF USE ONLY **Type of Search** **Vendors and cost where applicable**

a user.

A firmware has been mainly described above. However, when the device/unit is manufactured, a design department conducts a design relating to a hardware constituting the device/unit as well as a design relating to a firmware. Specifically, the design department makes various kinds of design drawings relating to the hardware such as a parent component drawing, a child component drawing, a logic circuit drawing, a printed circuit board packaging drawing, and a hardware test specification, and the like.

The above-mentioned parent component drawing shows a table of components of the device/unit and the child component drawing shows the constitution of the components described on the child component drawing. The logic circuit drawing shows a logic circuit of the device and the printed circuit board packaging drawing shows a packaging state when parts are mounted on a printed circuit board. The hardware test specification compiles specifications relating to various kinds of tests of checking the actions of the assembled device.

Design drawings and the like relating to the hardware will be called hardware components. Similarly, the various kinds of specifications relating to the firmware described above will be called firmware components. These hardware components and firmware components are separately managed under different rules in the management department and are distributed to

CON(1/5)

factories and the like when necessary. In the case where the hardware component or the firmware component is revised because of a change in design or the like, the management department manages the number of versions separately.

Concept

A client/server-type system has been conventionally used as a unit for managing the hardware components and the firmware components. This system is schematically constituted by a server placed in the management department and a plurality of clients placed in the factory and the like and accessible to the server via a network.

In the server are separately registered the hardware components and the firmware components. A client refers to the hardware components and the firmware components by using a browser. The client receives the hardware components and the firmware components via a network N. The operations relating to these reference and reception are performed by the operator of the client.

In the above-mentioned system, the place to which the hardware components and the firmware components are distributed (client) is limited by checking a password for the purpose of ensuring a security. In other words, in the conventional system, the place to which the hardware components and the firmware components are distributed is limited for each client by checking a pass word of the client.

To be specific, it is allowed to distribute specific

CON(7/5)

5), a ping command be sent to the reference-related client 30, the reception client 40, and the object machine 50 by the management server 10 to check the conditions of a communications line and that, in the case where the communications line of the object machine 50 is normal, the object machine 50 receive or refer to the component instead of the reference-related client 30 or the reception-related client 40. The object machine 50 is a high level machine above the reference-related client 30 and the reception-related client 40.

In the case where the communications line of the object machine 50 is abnormal and the communications lines of the reference-related client 30 and the reception-related client 40 are normal, it is also recommended that the reception-related client 40 or the reference-related client 30 receive or refer to the component.

motivation

As described above, since the hardware and the firmware are regarded as the same management level and a plurality of components related to both of the them are managed in a unified way, it is possible to improve the management efficiency of the version number of the components and the management efficiency of the components and to prevent a working error as compared with the conventional management in which components related to both of them are separately managed.

Further, as shown in Fig. 2, since the plurality of components constitute the hierarchical structure, it is

CON(3/5)

possible to easily take out the n-th layer component drawing from the first layer component drawing based on the meta-information by using the reference-related client 30 (or the reception-related client 40 or the object machine 50).

Further, since the meta-information F_1 shown in Fig. 4 comprises the content of the <WEB FILTER> tag, it is possible to take security measures related to the reception of or the reference to the component for extremely small unit of each component.

Further, since the component comprises the patch information and the patch processing is automatically performed by the reception-related client 40 side, it is possible to prevent a working error and to shorten working hours as compared with the conventional manual patch work.

Further, as shown in Fig. 2, since the plurality of components constitute the hierarchical structure, it is possible to easily retrieve a desired component from among the meta-information without separating the hardware from the firmware.

Further, in the case where the component is revised or in the case where a new component is registered in the component data base DB1, the reception-related client 40 or the reference-related client 30 can take out the applicable component in real time (or at an arbitrary time) when it receives the revised design notice (ECO) or the new design notice (NRN).

CON(4/5)

Accordingly, it is possible to prevent the omission of notice and to improve working efficiency because the client can take out the applicable component during the night time.

Further, since the management server 10 can conduct communications related to the development consignment of the product with the client 60 to which the development is consigned, it is possible to establish communications related to the development consignment, which results in shortening a period required to develop the product.

In addition, since the management server 10 conducts communications to get the permission of quoting the part catalog C with the vendor side client 70, it is possible to quickly get the permission of quoting the part catalog C.

motivation

Up to this point, while a preferred embodiment in accordance with the present invention has been described with reference to the drawings, it is not intended to limit the present invention to the specific constitution of the preferred embodiment, but the present invention may be further modified in design within the spirit and scope of the appended claims. For example, in the above preferred embodiment, it is also recommended that a component management program to realize the function of the management server 10 be recorded in a computer-readable recording medium 200 shown in Fig. 35 and that a series of management related to the components be performed by entering the component management program recorded in the

CON(5/5)

IN THE CLAIMS

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please **CANCEL** claims 3, 12, 13 and 17.

Please **AMEND** claims 1-2, 4-11 and 14-16 as follows.

1. (CURRENTLY AMENDED) A component management system comprising:

1-1 a storage unit storing hardware and firmware related ~~electronized~~electronic information components as a hardware and firmware component knowledge database, each ~~electronized~~hardware and firmware related electronic information component being ~~electronized~~electronic information generated during processes including ~~a product~~ design, development, manufacture, and inspection, of a product,

1-2 wherein the hardware and firmware ~~electronized~~related electronic information components include at least one of a drawing of a hardware constituting the product, a firmware, a program, a specification, and a contract for the product, as the ~~electronized~~electronic information,

* 1-3 wherein said hardware and firmware related electronic information components as a plurality of electronic information generated during the processes including the design, development, manufacture and inspection of the product constitute a hierarchical structure in which the hardware and firmware related electronic information components are stored according to a numbering system common to both hardware and firmware electronic information components and added to each hardware and firmware electronic information component,

* 1-4 wherein said storage unit stores meta-information according to Extensible Markup Language (XML) data expressing the hierarchical structure of the hardware and firmware related electronic information components, and

* 1-5 wherein said hardware and ~~said~~ firmware related electronic information components constituting said product are at a same management level;

a server which manages the hardware and firmware component knowledge ~~data base~~database stored in said storage unit; and

CLM (1/2)

1-6 at least one client, which is connected to said server via a network, ~~which~~ and takes out from said storage unit a ~~predetermined~~ desired hardware and firmware related electronic information component from ~~said storage unit via said network~~among said plurality of hardware and firmware related electronic information components constituting the hierarchical structure based on the meta information.

2. (CURRENTLY AMENDED) A component management device comprising:

a storage unit storing hardware and firmware related electronic information components as a hardware and firmware component knowledge database, each hardware and firmware related electronic information component being ~~electronized~~electronic information ~~that is~~ generated in processes ~~from~~including design, development, manufacture, and inspection, of a ~~product~~product,

wherein the hardware and firmware related electronic information components include at least one of a drawing of a hardware constituting the product, a firmware, a program, a specification, and a contract constituting the product, as the ~~electronized~~electronic information,

wherein said hardware and firmware related electronic information components as a plurality of electronic information generated during the processes including the design, development, manufacture and inspection of the product constitute a hierarchical structure in which the hardware and firmware related electronic information components are stored according to a numbering system common to both hardware and firmware electronic information components and added to each hardware and firmware electronic information component,

wherein said storage unit stores meta-information according to Extensible Markup Language (XML) data expressing the hierarchical structure of the hardware and firmware related electronic information components, and

wherein said hardware and ~~said~~ firmware related electronic information components constituting said product are at a same management level; and

a management unit managing the hardware and firmware component knowledge ~~data base~~database by controlling when a client takes out a desired hardware and firmware related electronic information component from ~~said storage unit via a network~~among said plurality of hardware and firmware related electronic information components constituting the hierarchical structure based on the meta information.

(LM (2/2)